TOPICAL REVIEW

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Topical Review

A review of III–V planar nanowire arrays: selective lateral VLS epitaxy and 3D transistors

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Abstract

Nanowires have long been regarded as a promising architecture for beyond Si CMOS logic, future III–V RF electronics, next generation optoelectronic applications, as well as heterogeneous integration. The inherent 3D structure also enables new device concepts that are otherwise not accessible with conventional technology. Nanowires grown using bottom-up epitaxial methods such as metalorganic chemical vapor deposition are free of ion-induced damage, which is especially critical for III–V because of the irreversibility of such damage, and can be scaled to dimensions smaller than lithographically defined. The challenges for nanowire based devices have been the controllability and compatibility with Si CMOS manufacturing. The discovery of parallel arrays of planar III–V nanowire growth mode provides an in-plane nanowire configuration that is perfectly compatible with existing planar processing technology for industry. The selective lateral epitaxy nature guided by the metal nanoparticles via the vapor–liquid–solid (VLS) mechanism opens up a new paradigm of crystal growth and consequently enabled *in situ* lateral and radial junctions. In this article, we review the planar nanowire based transistor development, particularly, planar III-As compound semiconductor based transistors enabled by this bottom-up self-assembled selective lateral VLS mechanism. We first review the characteristics and mechanism of planar nanowire growth, then focus on the growth, fabrication, and DC and RF performance of metal-semiconductor field-effect transistors, metal-oxide semiconductor field-effect transistors, and high electron mobility transistors (HEMTs), before providing our perspective on future development.

Keywords: nanowire, semiconductor, field effect transistor, III–V compound semiconductor, MOCVD, vapor–liquid–solid, HEMT

(Some figures may appear in colour only in the online journal)

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1. Motivation of 3D III–V nanowire transistors

Because of their high electron mobility and versatile heterojunctions, III–V compound semiconductors have not only enabled an entire optoelectronics industry and high-speed electronics, but are also well positioned for low power logic applications [1, 2]. Nanowires have long been regarded as a promising architecture for beyond Si CMOS logic and future III–V RF electronics, as well as next generation optoelectronic applications. In particular, nanowires grown using bottom-up epitaxial methods, such as metalorganic chemical vapor deposition (MOCVD) or molecular beam epitaxy (MBE), can be scaled to dimensions smaller than lithographically defined. The small dimension and non-planar 3D form factor allow strain relaxation through the sidewalls or multi-faceted free surfaces, which significantly relax the lattice match restriction for heterogeneous epitaxial integration.

The inherent 3D structure also enables new device concepts that are otherwise not accessible with conventional technology. For example, new logic field-effect transistors (FETs) now use 3D channels, including finFETs or gate-all-around (GAA)-FETs, for improved electrostatic control. These 3D channels are mostly formed by top-down etching methods such as reactive ion etching (RIE) without causing sustained damage to the sidewall facets. However, III–V semiconductors are significantly more susceptible to high energy ion damage that is difficult to repair, which makes forming III–V nanowire channels more challenging. Furthermore, forming heterojunctions that wrap around a 3D channel would require regrowth, where interface quality is extremely critical. Bottom-up growth methods, on the other hand, do not cause surface damage and are capable of monolithic 3D heterojunction formation by switching growth modes *in situ* from the axial to the radial direction of nanowires. Analogous to the holy grail of III–V integration on silicon substrates for digital applications, successful implementation of III–V nanowires on silicon will also impact radio frequency (RF) applications as high-speed, III–V heterojunctions on silicon are attractive from a cost perspective. Further, extreme heterogeneous integration such as III–V on flexible substrates could enable new devices for consumer wearable electronics or as lightweight, conformal communication devices [3].

The most widely reported process of semiconductor nanowire growth is the vapor–liquid–solid (VLS) [4, 5] or the relatively recent vapor–solid–solid (VSS) [6, 7] mechanism that involves a metal catalyst particle (externally supplied or *in situ* deposited [8]). The driving force for crystallization is the supersaturation of liquid or solid alloy droplets which are formed by metal catalytic capture of vapor phase reactants. The diameters of the nanowires are determined by the size of the metal catalyst seed particles, while the growth direction has largely been reported to depend on the surface free energy [9–11]. It has been shown that the lowest free energy surface is (1 1 1), and thus nanowires grown on (1 1 1) substrates are vertically aligned and perpendicular to the substrate [12] and those on (1 0 0) and (1 1 0) substrates are tilted out of plane at 35.3° and 54.7°, respectively. This bottom-up approach through metal-catalyzed growth allows for the routine synthesis of nanometer-scale devices and the flexibility to form functional heterostructures with materials that are otherwise incompatible due to large lattice constant mismatch. III–V semiconductor nanowires are of particular interest because of their direct bandgap, high carrier mobility, and ability to form versatile heterojunctions. To date, many classes of photonic and electronic devices have been demonstrated including electrically pumped lasers, light emitting diodes, photodetectors, FETs, and logic gates [13–19].

However, one of the key issues that needs to be addressed for practical applications is the integration of nanowire into devices and circuits with current planar processing technology. Current nanowire integration techniques generally include either, (1) the transfer of nanowires from the growth substrates to another substrate; or (2) the fabrication of devices with as-grown nanowires attached to the growth substrate. The first integration approach is desirable because highly lattice mismatched or even amorphous substrates can be used. For most research purposes, nanowires are randomly scattered onto a substrate and a scanning electron microscope (SEM) or optical microscope is used to isolate a single nanowire for device fabrication; this is clearly unsuitable for commercial applications. *Ex situ* assembly methods (micro-fluidics, electric field, magnetic field, etc) that are used to horizontally align and position individual nanowires have been explored with encouraging results but with limited wafer-scale success [20–24]. The second integration approach has been used to create highly uniform arrays of vertical nanowires through the patterning of metal catalyst on a nanowire growth substrate; however, the extremely high aspect ratio of the vertical nanowires is incompatible with existing processing technology.

The challenges for nanowire based devices have been the controllability and compatibility with Si CMOS manufacturing. Our discovery of parallel arrays of planar III–V nanowire growth mode provides an in-plane nanowire configuration that is perfectly compatible with existing planar processing technology for industry. The selective lateral epitaxy nature also opened up a new paradigm of crystal growth and consequently enabled *in situ* lateral junctions. We have previously provided a comprehensive review of controlling the nanowire growth direction [25]. In this article, we review the planar nanowire based transistor development, particularly, planar III-As compound semiconductor based transistors enabled by this bottom-up self-assembled selective lateral VLS mechanism. We first briefly review the mechanism of planar nanowire growth, then focus on the growth, fabrication, and DC and RF performance of metal-semiconductor field-effect transistors (MESFETs), metal-oxide semiconductor field-effect transistors (MOSFETs), and high electron mobility transistors (HEMTs), before providing our perspective on future development including integration on flexible substrates by transfer-printing.

2. Planar nanowire growth by selective lateral epitaxy

Vapor–liquid–solid growth [4] is one of the most popular methods used to synthesize semiconductor nanowires. The key is to use ultra-small metallic seed particles to direct the

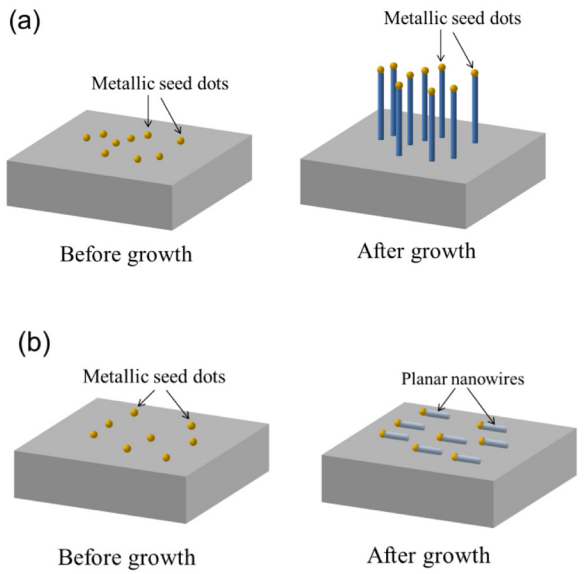

Figure 1. Schematic diagrams illustrating VLS nanowire growth. (a) Vertical VLS nanowires and (b) planar nanowires by SLE.

material growth in a self-assembly fashion. The apparatus used for growth is usually the same as those commonly used for bulk semiconductors, such as a MOCVD reactor or MBE system. At certain temperatures, the seed particle is converted to a supersaturated eutectic droplet containing the growth species, which come from the pyrolysis of vapor-phase precursors. As the growth species are continuously supplied, they precipitate out of the seed particle in the form of a solid, single-crystal semiconductor nanowire. This process is schematically shown in figure 1. The VLS growth in a MOCVD system usually takes place at a temperature lower than that of the conventional thin-film growth. The VLS growth can have a relatively high growth rate at low temperature thanks to the catalytic effect of seed particles in assisting the pyrolysis of growth precursors.

The commonly observed growth orientation of III–V VLS nanowires is ⟨1 1 1⟩B [25]. Vertically aligned nanowires can be obtained on a (1 1 1)B substrate. This is shown in figure 1(a). If a substrate with another surface orientation is used, titled nanowires are usually observed. By creating a (1 1 1)B vertical sidewall by etching a (1 1 0) or (2 1 1)B substrate, standing-alone ⟨1 1 1⟩ lateral nanowires can be grown [26]. The discovery of planar VLS nanowire growth [27] has totally changed this conventional picture where nanowires extend out of the substrate surface. Those planar nanowires do not usually follow a ⟨1 1 1⟩ direction. Instead, as shown in figure 1(b), they are self-aligned along certain in-plane crystalline directions, with their bottoms epitaxially attached to the substrate surface [27]. During the growth process, the seed particles move laterally on the substrate surface and leave a semiconductor nanowire in its trace. We name this particular kind of VLS growth selective lateral nano-epitaxy (SLE). Different from the conventional selective area growth of lateral structures where the selectivity is realized by patterned hard mask (SiO_2 for example) [28–30] and the growth direction is normal to the substrate surface, the area selectivity in SLE is provided by the seed particles and the growth occurs in parallel with the surface. Recently, lateral growth of InAs nanowires on an HSQ mask surface has been observed in a selective area growth on a GaAs substrate [31]. However, the precise control of yield and nanowire morphology has been challenging. Another interesting but different approach for selective area growth of lateral III–V nanowire is to confine the growth in a horizontal SiO_2 tube created by etching the core Si [32].

2.1. Homoepitaxy of GaAs planar nanowires

The initial studies of SLE after its first discovery were carried out on homoepitaxy of GaAs planar nanowire on GaAs substrates [27, 33–35]. Those studies have provided some very fundamental understanding of this particular type of growth. All of our nanowire growth experiments were performed in an Aixtron MOCVD 200/4 reactor. The standard homoepitaxy of GaAs planar nanowires started with an oxide-desorption annealing with AsH_3 overpressure at 625−650 °C for 10 min. The reactor temperature was then ramped down to the target nanowire growth temperature, normally between 440–480 °C. After temperature stabilization, the TMGa precursor was introduced to start a timed nanowire growth. Finally, the samples were cooled usually under AsH_3 overpressure.

2.1.1. Orientation. Our early results showed that the planar GaAs nanowires grown on GaAs (1 0 0) substrates had a bi-directional feature [27]. The nanowires chose two growth directions that are antiparallel to each other: [0 −1 1] and [0 −1 −1]. Further studies suggested a universal law—planar nanowire growth follows the projections of out-of-plane ⟨1 1 1⟩B directions on the substrate surface [33, 36]. Note that ⟨1 1 1⟩B is the predominantly observed III–V nanowire growth direction. On a (1 0 0) substrate, there are two available out-of-plane ⟨1 1 1⟩B directions whose surface projections are [0 −1 1] and [0 −1 −1], respectively. On a (1 1 0) substrate, there is only one available ⟨1 1 1⟩B direction so unidirectionally aligned nanowires can be achieved [33]. This is schematically shown in figure 2 with example SEM images. The projection theory has been further verified on a (1 0 0) wafer with 10° offcut toward [0 −1 0]. The growth directions predicted by the projection theory closely match the characterization results from x-ray microdiffraction [36].

2.1.2. Growth rate. For homoepitaxy of GaAs planar nanowires, the growth temperature window is from 440–480 °C for constant temperature growth. For temperature lower than 440 °C, most nanowires tend to take off from the substrate at the beginning of the growth, resulting in tilted nanowire array. For temperature higher than 480 °C, the normal vapor–solid thin-film deposition becomes significant, leading to very tapered planar nanowires. A similar temperature effect was also seen on planar GaAs nanowire growth on a (3 1 1)B substrate [37]. By doing a two-temperature-step growth to improve planar nanowire quality, the final temperature can reach lower than 440 °C while the nanowires remain planar [34]. The growth rate of planar nanowires can be extremely high (close to 100 nm s^{-1}) in the temperature range mentioned above. Within

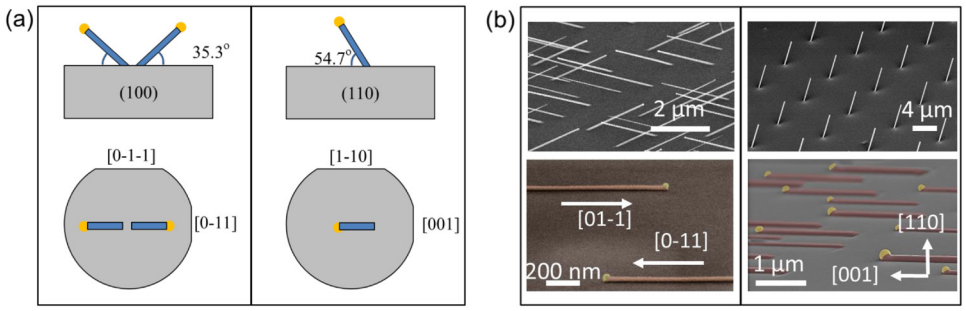

Figure 2. (a) Schematic diagrams showing the relationship between planar nanowire growth directions and out-of-plane growth directions. The left shows growth on a (1 0 0) substrate and the right shows the (1 1 0) case. (b) SEM images that correspond to each case in (a). (b) © 2012 IEEE. Reprinted with permission from [27, 33]).

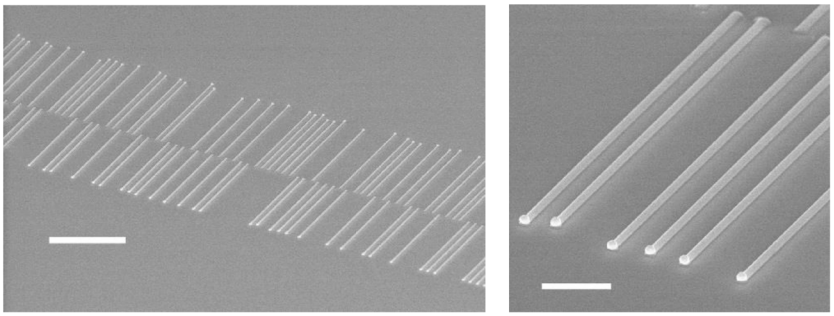

Figure 3. SEM image of a large-scale planar GaAs nanowire array on (1 0 0) GaAs with perfect yield (left). A magnified image is shown on the right. The scale bars are 5 and 1 μm, respectively. Reprinted with permission from [35]. Copyright 2014 American Chemical Society.

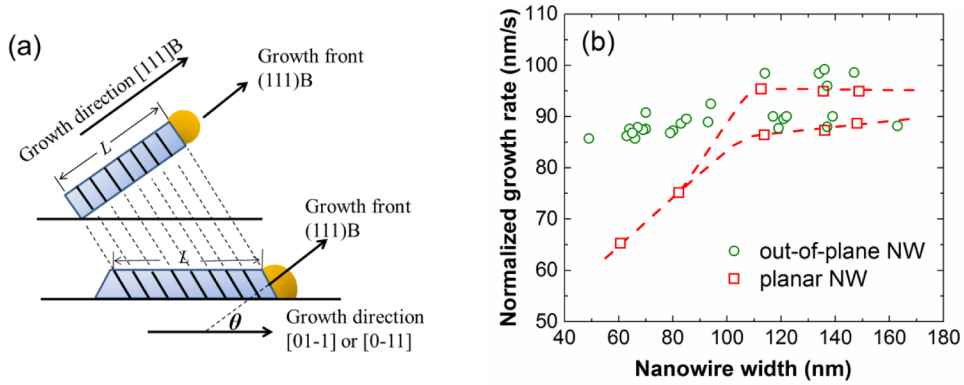

Figure 4. Growth rate comparison between planar and out-of-plane nanowires. (a) Schematic diagrams showing growth front and growth direction. (b) Comparison between normalized growth rates. The growth was done at 460 °C with a V/III ratio of 30. This growth condition leads to the appearance of both planar and out-of-plane nanowires. The dashed lines are only there to guide the eyes. Reprinted with permission from [35]. Copyright 2014 American Chemical Society.

certain appropriate growth parameter space including optimized V/III ratio and growth rate, the ratio between the planar nanowire VLS growth rate and thin-film vapor–solid growth rate can be more than three orders of magnitude [34].

Our early works on planar nanowire growth have been done with dispersed colloidal Au as seed particles. This is a very convenient way of obtaining various nanowire diameters. Later, we developed a method of realizing array-based planar nanowire growth with Au seed dot arrays patterned by electron beam lithography and a standard lift-off process. This is toward large-scale manufacturing of aligned nanowires. In order to ensure the planar growth mode, the substrate surface needs to be pristine—completely free of any trace amount of contaminates such as polymer residues from chemical resist used in lithography patterning. This is achieved by prolonged solvent cleaning with sonication followed by a native oxide removal etch with HCl. The cleaning process is so critical that otherwise no consistent growth results can be obtained (i.e. many out-of-plane nanowires appear). From the array-based SLE, we found that the yield of planar nanowires is highly dependent on the V/III flow ratio used during growth. A V/III of around 1 has repeatedly led to the perfect yield of planar nanowire array growth. Figure 3 shows an example of a massively aligned planar nanowire array which is suitable for practical device applications.

Based on the array-based SLE, we have done studies aimed at understanding the SLE growth mechanism. Figure 4 shows a comparative study of the growth rate of planar nanowires and out-of-planar nanowires on (1 0 0) substrates. In order to

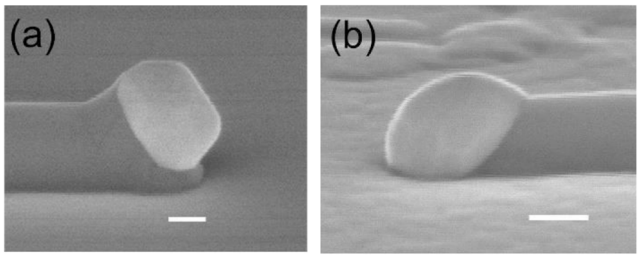

Figure 5. SEM images showing the shapes of seed particles after growth. (a) Sample cooling with AsH_3 overpressure and (b) without AsH_3 overpressure. The scale bars are both 100 nm. Reprinted with permission from [35]. Copyright 2014 American Chemical Society.

do a fair comparison, a normalized grow rate $R_n = R_m\cos\theta$ is used, where θ is the angle between the growth front and growth direction as illustrated in figure 4(a) (0° and 35.3° for out-of-plane and planar nanowires, respectively). The normalized growth rates versus nanowire width are shown in figure 4(b). Each data point of the planar nanowires is an averaged number from a planar nanowire array. Each data point of the out-of-plane nanowires is measured from single nanowires (only a few out-of-plane nanowires seen in this growth condition are used). Note that a slight difference in growth rate is seen between the [0 1 −1] and [0 −1 1] directions for $D > 100$ nm. It is interesting to see that for relatively large nanowires, the growth rates of planar and out-of-plane nanowires match closely. However, planar nanowire growth rate rolls off much faster as the width shrinks. Based on the conventional VLS model from Givargizov [38], this trend implies that planar nanowires are more vulnerable to the Gibbs–Thomson effect and have less supersaturation at smaller width.

2.1.3. Growth mechanism. Shown in figure 5 are SEM images of the seed particles. In a standard growth recipe, when planar nanowire growth is finished, Ga precursor (TMGa) is turned off followed by a cooling step with AsH_3 overpressure. As there is a substantial amount of Ga in Au seed particle during growth, an additional segment of GaAs is formed during the cooling process leading to a neck-like structure behind the seed (figure 5(a)). When we turned off AsH_3 during cooling, the original shape of seed particles during nanowire growth was preserved (As solubility in Au is very low). This is shown in figure 5(b) where we see a direct interface between the particle and the GaAs substrate. We therefore suggest that it is the adhesion energy between the seed particles and substrate that prevents the nanowire growth from taking off from the substrate surface and reaching the more energetically favorable out-of-plane growth mode. We speculate that the wetting process happens at the very beginning of the growth during the oxide desorption step. During nanowire growth, the seed particle moves horizontally with its bottom surface in contact with the substrate. To reach the out-of-plane mode, the adhesion needs to be overcome. The importance of this is that it implies that the planar growth or SLE could be universal to any materials and not limited to homogeneous growth as long as the adhesion between the seed particle and substrate is strong enough and the substrate surface orientation is not the same as the growth front.

2.1.4. Density of planar nanowires by SLE. It is critical to pack as many as possible nanowires per area in the channel in order to increase on-current and reduce parasitic capacitance resulting from the gaps in-between the nanowires for high-speed operation. The planar nanowires formed by SLE are self-aligned and perfectly parallel along a particular crystal orientation, therefore there is practically no limit on how close they can be placed. The only practical limit is how dense the Au catalyst particles can be patterned. As shown in figure 6, nanowires as close as 15 nm (figure 6(a)) or 85 nm (figure 6(b)) were realized by simply growing them from randomly dispersed Au catalyst nanoparticles.

2.2. Heteroepitaxy of InAs planar nanowires on GaAs substrates

InAs is a lower bandgap III–V material and has a higher electron mobility than GaAs [1]. There is a lot of interest in InAs and high-In-content InGaAs material for future ultra-low power CMOS applications at ~0.5 V V_{dd} [1, 2, 39–42]. Growth of thin-film InAs is usually difficult because commonly available III–V substrates such as GaAs and InP are significantly lattice-mismatched to InAs. The lattice mismatch between InAs and GaAs is ~6.7%. The theoretical prediction of the critical layer thickness for dislocation-free growth of InAs on GaAs is in the range of 3–8 monolayers [43–45]. Experimentally, a strain-induced transition from 2D growth to 3D growth was observed after about only two monolayers [46–49]. Direct growth of vertical nanowires can usually accommodate larger lattice mismatch as compared to thin-film growth [50]. Regarding InAs nanowires, there have been studies on vertical VLS growth [51, 52], vertical SAE growth [53, 54], and direct vertical growth [55] on foreign substrates. Nonetheless, as mentioned before, vertical nanowires are not quite suitable for practical application due to the incompatibility with the standard planar process technology.

Following the same VLS planar growth concept, we have demonstrated the heteroepitaxy of a self-aligned InAs nanowire directly on a GaAs substrate [35]. The planar InAs nanowire growth takes place at a lower temperature (340–360 °C in this study), in contrast to ~440–460 °C for planar GaAs nanowire growth. Figure 7(a) shows a SEM image of two parallel planar InAs nanowires on a semi-insulating GaAs (1 0 0) substrate. The high resolution (HR) TEM image in figure 7(b) confirms the nanowire, ~12 nm in height, is single-crystalline and appears to be free of stacking faults and interfacial dislocations (at least low in density that is not easily detected). The inset in figure 7(b) shows the fast Fourier transform (FFT) pattern of the HR-TEM image, indicating cubic symmetry and thus the epitaxial relationship with the substrate. The FFT pattern also shows coincident spot splitting, with the inner (outer) spots associated with the InAs nanowires (GaAs substrate), as labeled. The spot splitting indicates that the nanowire is

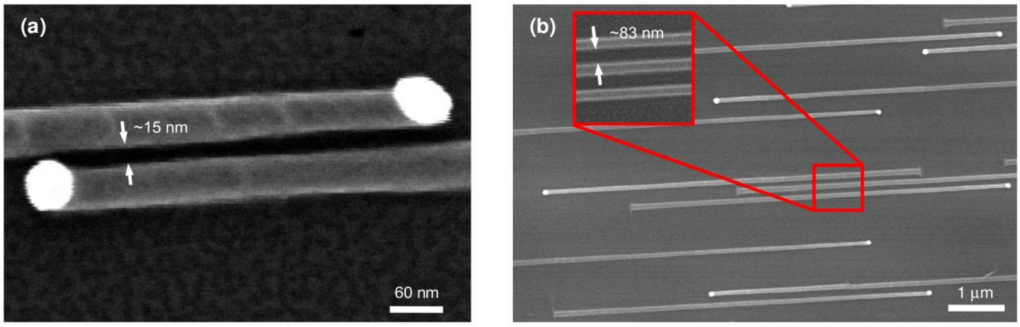

Figure 6. Planar GaAs nanowires grown by SLE from randomly dispersed colloidal Au nanoparticles with close spacing between the nanowires: (a) 15 nm and (b) 83 nm spacing.

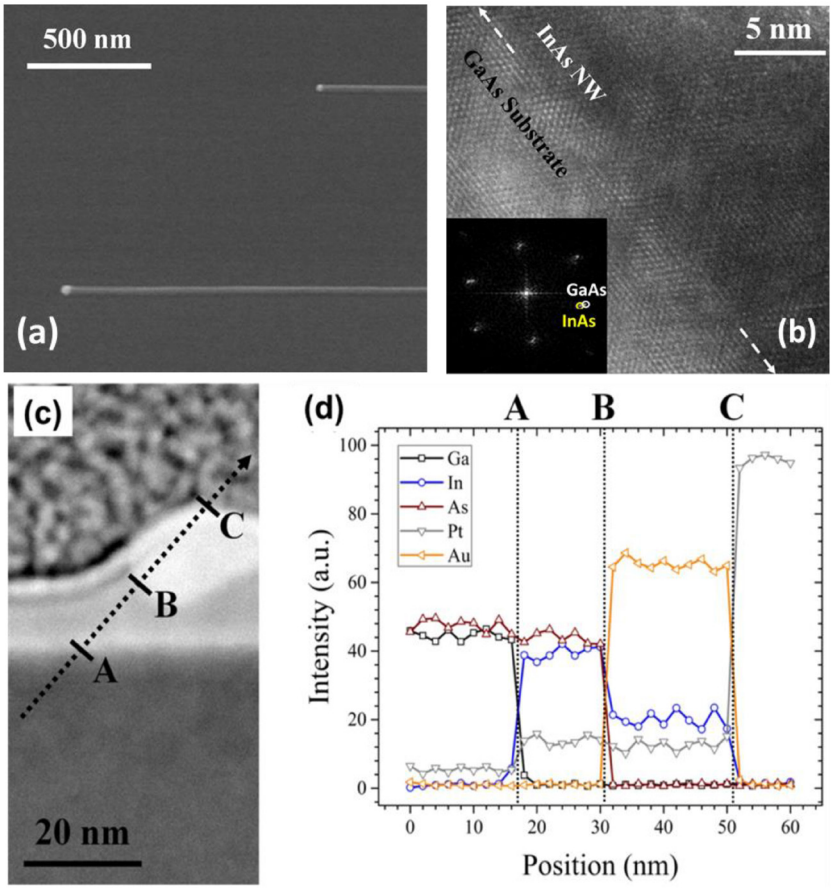

Figure 7. (a) Tilted-view SEM image showing two self-aligned VLS planar InAs nanowires on a GaAs substrate. (b) Cross-sectional HRTEM image of the planar InAs nanowire and GaAs substrate interface, with the inset showing the FFT pattern where the split diffraction spots for GaAs and InAs are as labeled. (c) HAADF-STEM image showing the tip, including the Au particle, of a heteroepitaxial planar InAs nanowire on GaAs substrate. (d) EDXS line-scan collected along the location of the black dotted line in (c). Reprinted with permission from [35]. Copyright 2014 American Chemical Society.

indeed relaxed to some extent. Figure 7(c) shows an example HAADF-STEM image of the InAs planar nanowire tip on a GaAs substrate. From the EDXS line scan shown in figure 7(d), we can clearly identify the GaAs substrate, InAs nanowire body, and the Au seed particle. Clearly, with an ~7% lattice mismatch, the thickness of the InAs planar nanowire is well above the thin-film InAs critical thickness on GaAs. Even with the planar configuration, nanowires still possess significantly enhanced strain accommodation capability compared to planar thin films. We attribute this capability to the small diameter and height of the InAs nanowire, where the mismatch strain is presumably relaxed through the free surfaces (top and sidewalls).

2.3. Radial heterojunctions in planar nanowires

As discussed above, there is a preferred temperature window for planar nanowire growth (e.g. 440–480 °C for planar GaAs nanowires). When the reactor temperature is raised very high (e.g. above 600 °C), the dominant growth would be the normal vapor–solid thin-film growth. At such high temperature, the catalytic effect of seed particles for precursor pyrolysis

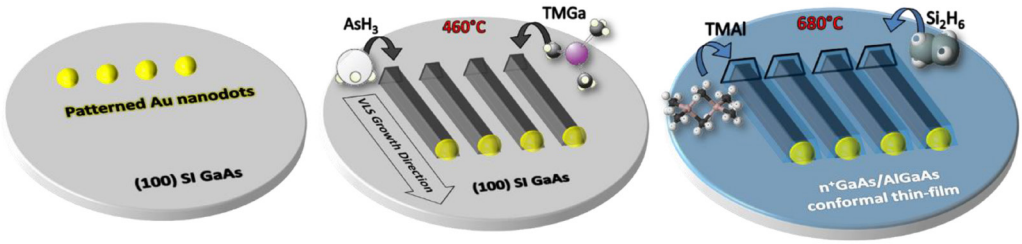

Figure 8. Illustration of core–shell heterojunction AlGaAs:Si/GaAs formation in a planar nanowire array, using TMGa, AsH_3, TMAl, and Si_2H_6 as MOCVD precursors of Ga, As, Al, and Si, respectively.

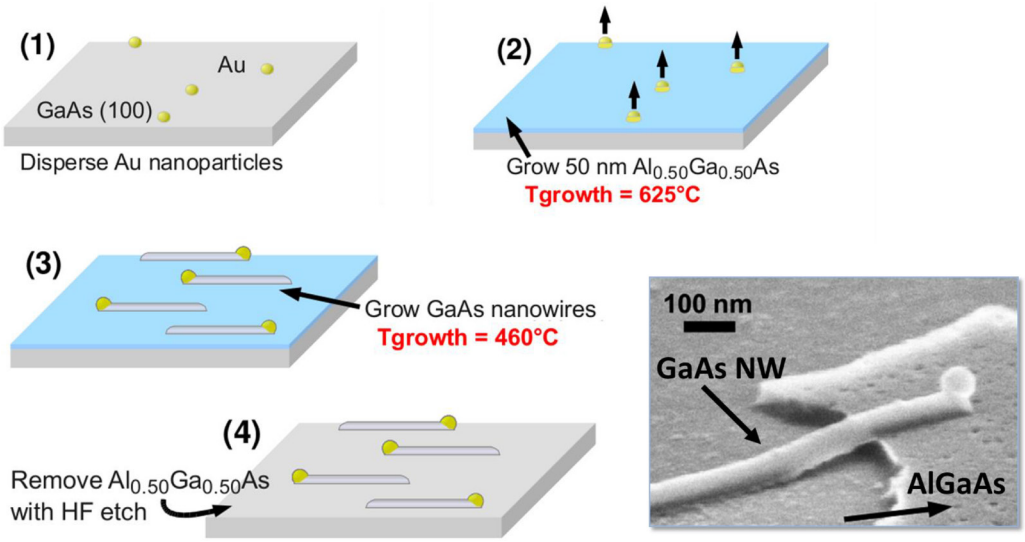

Figure 9. Illustration of the process of inserting an AlGaAs sacrificial layer for planar GaAs nanowire growth monolithically, with randomly dispersed Au nanoparticle seeds (apply also to patterned Au seeds): (1) place Au nanoparticles on a (1 0 0) GaAs substrate, (2) grow a 50 nm AlGaAs sacrificial layer at growth temperature of ~625 °C, while the Au nanoparticles are automatically elevated to the top of the surface, (3) lower growth temperature to ~460 °C and adjust V/III ratio to grow planar GaAs nanowires, and (4) remove the AlGaAs sacrificial layer by etching in HF to release the planar GaAs nanowires from chemically bonding to the substrate, to be ready for liftoff. The SEM image shows a partially released planar GaAs nanowire as the AlGaAs layer is removed. Reprinted with permission from [27]. Copyright 2008 American Chemical Society.

diminishes because the pyrolysis of precursors is efficient even without the help from seed particles. Furthermore, the VLS growth would be suppressed due to less available growth element in seed particles and larger content of growth element required to reach supersaturation. Thus, we can use the growth temperature to switch between VLS planar nanowire growth mode and vapor–solid thin-film growth mode and form a planar GaAs nanowire core–shell heterostructure [34, 56, 57]. Figure 8 illustrates the growth of the planar GaAs nanowire (core)/AlGaAs thin-film (shell) heterostructure. First, VLS planar GaAs nanowire growth is initiated at a growth temperature of 460 °C with trimethyl-gallium (TMGa) and AsH_3 as the growth precursors. Then, the growth temperature is raised to 680 °C, which suppresses the VLS planar nanowire growth and promotes the vapor–solid thin-film growth. With additional flows of trimethyl-aluminum (TMAl) and Si_2H_6, n-type AlGaAs thin film would be grown on top of the trapezoidal planar GaAs nanowires. Such planar nanowire core–shell heterostructure can be utilized for nanowire surface passivation and for making planar nanowire based HEMTs which will be shown in detail in section 5 [34, 56–58].

2.4. Heterogeneous integration by epitaxial liftoff

For RF applications, discrete 3D channel nanowires have a distinct advantage over planar III–V materials for pick-and-place printing and integration onto flexible and cost-effective rigid substrates. To facilitate this, the nanowires must assemble on an engineered epitaxial GaAs layer with an underlying sacrificial layer instead of using the bulk GaAs substrate. Fortunately, very good etch selectivity exists in the $Al_xGa_{1-x}As$ where for $x >$ ~0.45, a stark contrast in HF-based wet-etching is observed with binary AlAs etching very quickly while binary GaAs is extremely stable. However, AlGaAs readily oxidizes in air so that Au seed nanoparticles for SLE via Au-assisted VLS mechanism cannot be patterned on a AlGaAs template directly.

Two approaches have been attempted to incorporate a AlGaAs sacrificial layers in nanowire SLE for post-growth epitaxial liftoff. In the first method, the Au seed particle patterning is simply done on a GaAs substrate as usual and an AlGaAs layer is grown under vapor–solid growth mode that results in thin-film growth while the Au nanoparticles elevate to the top of the surface. Growth then switches to the VLS mode

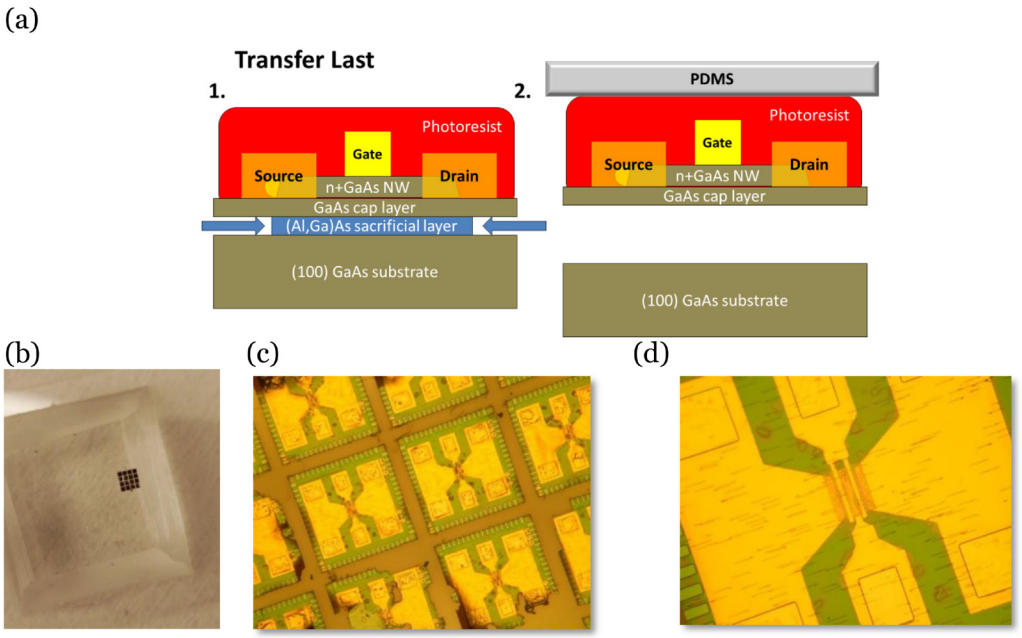

Figure 10. (a) Illustration of transfer last process. The nanowire FET is fully fabricated on the top side, then covered with photoresist (1). Then, the (Al, Ga)As layer is selectively wet-etched in HF:ethanol (2:1) to release the nanowire FET. With the device weakly tethered to the wafer with photoresist, a PDMS stamp is then applied and peeled back to break the resist bond (2). (b) 4 × 4 array of nanowire FETs released from the GaAs substrate and picked up using a PDMS stamp. (c) The 4 × 4 array of devices printed and released from the PDMS stamp onto an adhesive-coated glass wafer piece. (d) Zoom-in view of a successfully transferred nanowire FET prototype in (b). Adapted from Chabak (2016 *Thesis* University of Illinois).

to allow for GaAs nanowire growth directly on the AlGaAs layer just deposited *in situ*. Figure 9 illustrates the monolithic AlGaAs sacrificial layer incorporation and releasing scheme and shows partially released planar GaAs nanowires using this method. Note that the self-aligned planar nanowires can only be grown on high quality single crystal substrates and amorphous substrates will lead to out-of-plane randomly oriented nanowires. The *in situ* deposition of AlGaAs without exposing to air is critical to ensure that the template for nanowire growth is single crystal in nature. Once released, the nanowires will only be attached to the substrate by van der Waals force. Remarkably, releasing the nanowires by this method does not disturb the nanowire alignment, probably because of the strong surface tension. As a result, well-aligned arrays of planar nanowires can now be pick-and-placed onto arbitrary substrates for heterogenous integration while maintaining both the alignment and registry, as shown in [26].

The above approach works well only for $Al_xGa_{1-x}As$ where $x \leqslant 0.5$; higher Al composition AlGaAs degrades the selectivity of planar nanowire epitaxy. The second approach is to grow a template with the AlGaAs sacrificial layer embedded underneath a GaAs cap layer before the Au seed particle patterning. We investigated the quality of GaAs nanowire grown on varying thicknesses of the $Al_xGa_{1-x}As$ (x ~ 0.45–0.7) sacrificial layer in the range of 20–500 nm and the GaAs cap (~10–50 nm) templates grown by MOCVD on (1 0 0) GaAs substrates. As expected, thicker AlGaAs layers cause surface roughness which results in out-of-plane nanowire growth or planar nanowires with peculiar right-angle turns in plane. Optimum planar nanowire growth was observed on the thinnest (~20 nm) epitaxial low Al% composition AlGaAs layers with a GaAs cap of 10–20 nm in thickness.

To release GaAs nanowires from the native substrate for device fabrication on a foreign substrate, the nanowires can be transferred before metal contacts as mentioned above. In addition, transfer last (TL) after complete top-side fabrication is also feasible. The TL process shields the nanowires from chemicals, but the FETs and contacts can be susceptible to cracking, etc. The TL process is shown in figure 10(a). The nanowires are self-assembled on the engineered sacrificial epitaxial template and front-side FET fabrication is completed. Then, the entire sample is submerged in a two-step wet-etch followed by patterning a photoresist box on the entire FET to protect it from wet-etching. The first wet-etch is H_3PO_4:H_2O_2:H_2O (25:3:1) to etch away the GaAs cap layer and reveal the (Al,Ga)As sacrificial layer on the perimeter of the box. The box pattern mask is removed in acetone, and the sample is re-patterned with photoresist corner anchors to keep the FET from floating away in the next etch steps. The sample is immediately cleaned in H_2O and submerged in a 2:1 HF:ethanol solution to remove the small amount of AlGaAs sacrificial layer. The ethanol acts as a surfactant to mitigate the 'bubbling' which can create a self-seal around the sample preventing HF etching [59]. Finally, a stamp or adhesive was used to pick up the device. Figure 10(b) shows a 4 × 4 array of nanowire FET devices on a PDMS stamp after picking up the devices from the GaAs substrate. Figure 10(c) shows an optical image of transferred devices. An adhesive, a UV-curable polymer, was spun and baked at 110 °C for 20 min on a receiver glass substrate so the adhesion force was enough to release the PDMS stamp after printing the device. The stamp was gently pressed against the adhesive coated glass substrate and slowly lifted back to reduce damage of the nanowire devices. Each printed device is approximately

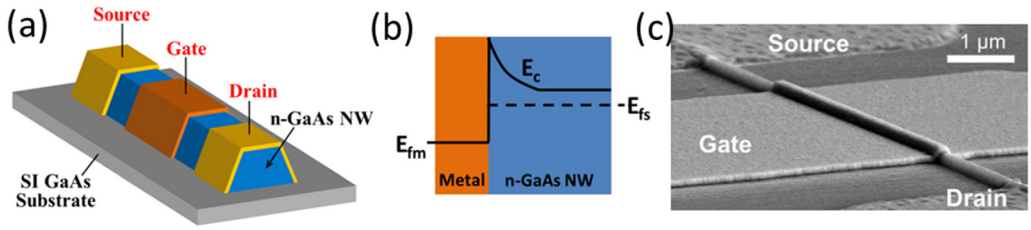

Figure 11. (a) Schematic illustration of a planar GaAs nanowire MESFET. (b) Band diagram across the gate region at the 'ON' state. (c) Tilted SEM image of a planar ⟨1 1 0⟩ GaAs nanowire MESFET on a SI (1 0 0) GaAs substrate with $L_g \sim 4$ μm and source-to-drain separation $L_{sd} \sim 8$ μm. © 2009 IEEE. Reprinted, with permission, from [60].

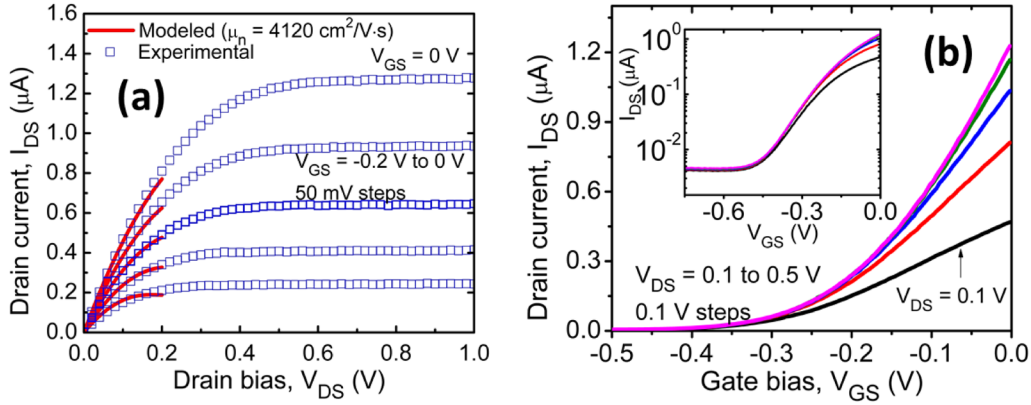

Figure 12. DC characteristics of a planar GaAs nanowire MESFET. (a) Output characteristics of the device as shown in figure 11(c) with V_{gs} stepped from −0.2–0 V in 50 mV step. Symbols represent experimental data while the solid red lines represent fitted data from a long-channel MESFET model by setting μ_e to be 4120 $cm^2\ V^{-1} \cdot s^{-1}$. (b) Transfer characteristics of the device as shown in figure 11(c) with V_{ds} stepped from 0.1–0.5 V. © 2009 IEEE. Reprinted, with permission, from [60].

400 × 400 μm. While a few of the devices were transferred neatly, there were several in figure 10(c) that were damaged and would benefit from an automated transfer printing process with delicate and repeatable mechanical pick and place force.

3. Planar GaAs nanowire MESFETs and simple circuits

A MESFET utilizes a metal-semiconductor Schottky gate to modulate the depletion width and to tune the conductance of a doped semiconductor channel. A MESFET with a doped nanowire channel would benefit from enhanced gate electrostatic control and have higher transconductance and better switching characteristics. Using Si-doped planar GaAs nanowires grown on a semi-insulating (SI) GaAs substrate as the channel and a metal-GaAs Schottky junction as the gate, our group has successfully made planar GaAs nanowire MESFETs [33, 60]. However, there are still challenges regarding on how to dope VLS planar nanowires controllably and uniformly [61–63].

As illustrated in figures 11(a) and (b), the metal-GaAs Schottky gate can modulate the depletion width in the doped planar GaAs nanowire, and thus tune the conductance of the planar GaAs nanowire. Figure 11(c) shows a planar ⟨1 1 0⟩ GaAs nanowire MESFET on a SI (1 0 0) GaAs substrate with gate length (L_g) ~4 μm and source-to-drain separation (L_{sd}) ~8 μm. Figures 12(a) and (b) show the output and transfer characteristics of the device as shown in figure 11(c). Assuming that the doped planar GaAs nanowire is fully depleted when the gate bias (V_{gs}) is at the threshold voltage (V_t) and by solving the Poisson equation of the trapezoidal nanowire cross-section, the doping level of the planar GaAs nanowire was extracted to be 2×10^{17} cm^{-3}. By fitting the linear regime of the output *I–V* curves with a standard long-channel MESFET model, the electron mobility (μ_e) of the nanowire was extracted to be 4120 $cm^2\ V^{-1} \cdot s^{-1}$. Figure 12(a) shows excellent agreement between the model with μ_e set to 4120 $cm^2\ V^{-1} \cdot s^{-1}$ (red lines) and the experimental data (symbols). The extracted μ_e at the extracted doping level agrees very well with the reported bulk GaAs mobility [64], which indicates that the planar GaAs nanowires have excellent crystal quality.

A further demonstration of the functionality of the doped nanowires was the formation of a simple version of a circuit [65]. This was also a step forward to show the manufacturability of the SLE technique. As shown in figures 13(a) and (b), a current-source loaded amplifier is formed by interconnecting planar GaAs nanowire MESFETs. Those devices are made on uni-directionally aligned GaAs planar nanowires grown on (1 1 0) SI substrate and n-type doped by Si. The SI substrate serves for device isolation. Shown in figure 13(c) is the electrical output versus input characteristics of the amplifier. A high peak voltage gain of 120 was achieved. We attribute this high voltage gain to the high output resistance resulted from the gate electrostatic improvement in the tri-gate nanowire structure.

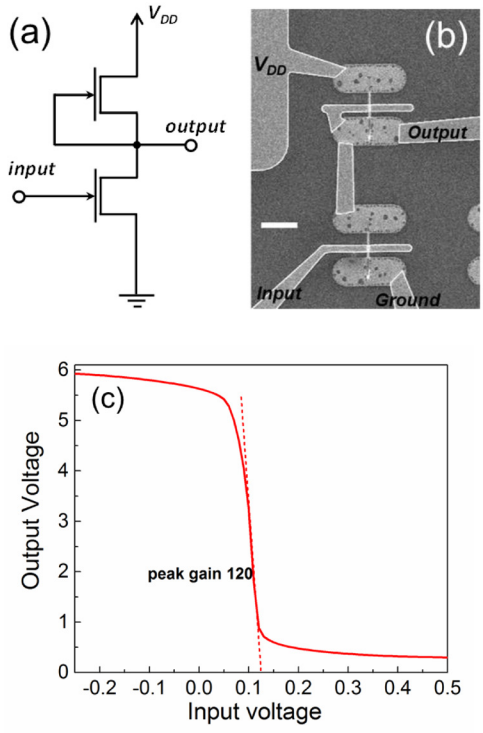

Figure 13. Demonstration of a simple current-source loaded amplifier by interconnecting individual planar nanowire MESFET. (a) Schematic circuit diagram. (b) A SEM image of the planar nanowire circuit. Scale bar is 4 μm. (b) Output versus input characteristics. © 2013 IEEE. Reprinted, with permission, from [65].

4. GaAs and InAs planar nanowire MOSFETs

In our early work, MOSFET operation was demonstrated on a homogeneous planar GaAs nanowire (tri-gate) with decent performance that is comparable to planar GaAs MOSFETs [66]. Heterogeneous InAs planar nanowire MOSFETs have also been developed by our group [67, 68]. Owing to the exceptionally high electron mobility in InAs, InAs nanowire transistors have been extensively studied in the literature. Those devices are mostly based on dispersed [69–75] and vertical InAs nanowires [76–80]. Our heterogeneously grown planar InAs nanowires hold the potential for large-scale integration, but there are process challenges regarding how to turn them into GAA structures.

In order to achieve a GAA structure, we released the InAs planar nanowire from the GaAs substrate by selectively etching GaAs material. During the nanowire growth, an ultra-thin layer of InAs film was simultaneously deposited on the substrate via the vapor–solid growth mode. This film not only contributes to excessive off-state leakage but also blocks the etchant from accessing GaAs underneath. This film was removed in a controllable way by digital etch [81] before nanowire release. The final device structure is schematically shown in figure 14.

Figure 15 shows SEM images of InAs nanowire devices. Shown in figure 15(a) is a nanowire hanging over a GaAs trench after the release etch. A final device structure is shown in figure 15(b). Figure 15(c) shows a cross-section image where gate metal is wrapping around the nanowire. It has to be mentioned that without releasing the nanowire, the device shows high conductivity and cannot be turned off. This is

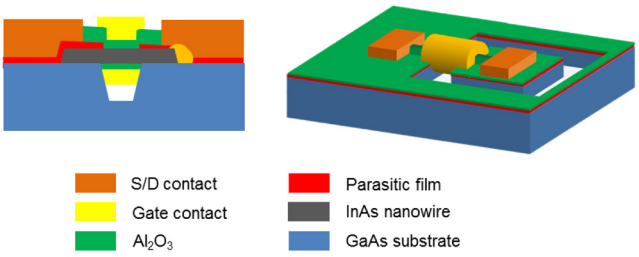

Figure 14. Schematic diagrams illustrating the fabricated InAs planar nanowire MOSFET device. The left shows the cross-section along channel direction and the right shows a tilted view.

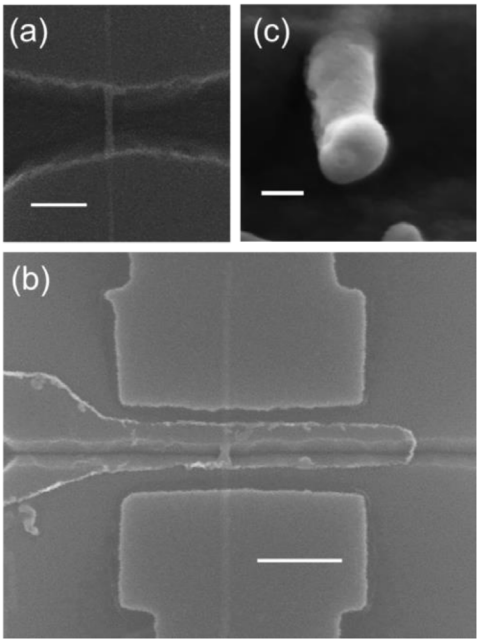

Figure 15. (a) SEM image showing a long InAs nanowire on a GaAs trench. (b) SEM image of a short channel device with S/D contacts at the top and bottom, and the gate finger in the middle. (c) Cross-sectional SEM image of a device after focused ion beam (FIB) cut. Scale bars are 300 nm, 400 nm and 50 nm for (a), (b) and (c), respectively. © 2015 IEEE. Reprinted, with permission, from [67].

shown in figure 16(a) where the dashed line represents a device applied with digital etch but with no release etch. After performing nanowire release, the on-off ratio as shown by the solid lines can be improved to as high as 10^4. It is speculated that the leakage current is caused by surface Fermi level pining at the bottom interface between InAs and GaAs. In this sense, the gate length here, as shown in figure 14, is determined by the releasing trench width on GaAs, not the gate metal width.

The electron mobility in our planar InAs nanowires as estimated from the long-channel device ($L_g = 350$ nm) [67] is 2730 $cm^2\ V^{-1} \cdot s^{-1}$. This is to be compared with the typical electron mobility in Si inversion layer (several hundred in $cm^2\ V^{-1} \cdot s^{-1}$ [82]). Figure 16(b) shows our recent results of a down-scaled device with gate oxide (ALD Al_2O_3) thickness reduced to 4 nm and gate length shrunk to 75 nm. This device exhibits a width-normalized peak extrinsic transconductance of ~830 mS mm^{-1} at $V_{ds} = 0.5$ V and a drive current of ~400 mA mm^{-1} at 0.5 V overdrive. Those are significantly improved from our long-channel device reported previously.

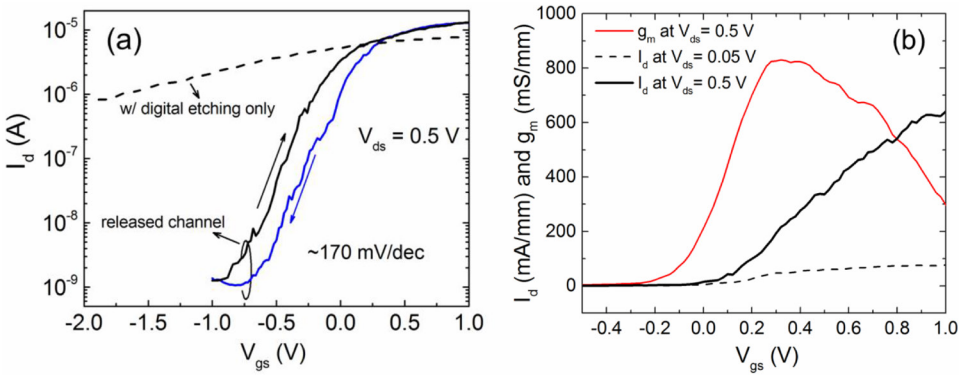

Figure 16. (a) Comparing the transfer curves of InAs planar nanowire MOSFETs with and without channel release. © 2015 IEEE. Reprinted, with permission, from [67]. (b) Transfer and transconductance characteristics of a short-channel InAs planar nanowire MOSFET with $t_{ox} = 4$ nm, nanowire width $d = 22$ nm and gate length $L_g = 75$ nm. The data is normalized by nanowire width.

5. Planar GaAs nanowire HEMTs

III–V HEMTs are the preferred platform for RF applications because of the high electron velocity in the undoped channel over doped MESFETs and MOSFETs. For nanoscale devices, the doping aspect makes HEMTs even more advantageous because it avoids the statistical variability of discrete random dopants in nanoscale channels. Therefore, it is highly desirable to adopt a version of the 3D MOSFET using a HEMT structure for high-frequency RF performance.

The motivation behind 3D transistors overwhelmingly favors static over analog performance. This is driven mainly by the intrinsic gain of a 3D transistor expressed as

$$G_o = \frac{G_M}{G_{DS}} \quad \text{(unitless)} \tag{1}$$

where G_M is the DC transconductance (dI_{DS}/dV_{GS}) and G_{DS} is the DC output conductance (dI_{DS}/dV_{DS}). In short, a wrap-gate 3D transistor channel has improved short-channel effects (lower G_{DS}) without sacrificing G_M. However, very little has been reported about the high-speed performance of 3D transistors because of the high-density packing of 3D channels required to reduce parasitic capacitance. While a 3D geometry improves DC performance, the unused space between adjacent fins forms a parasitic capacitance between the gate, source and drain terminals. The current-gain cutoff frequency for assessing high-speed potential can be expressed in many forms expressing inverse time delay as follows:

$$f_T = \frac{1}{2\pi}\left(\frac{1}{\tau}\right) = \frac{1}{2\pi}\left(\frac{v_{eff}}{L_G}\right) = \frac{1}{2\pi}\left(\frac{G_M}{C_G}\right) \quad \text{(Hz)} \tag{2}$$

where τ, v_{eff}, G_M and C_G are the channel transit time, effective electron channel velocity, transconductance and gate capacitance, respectively. In a 3D channel array FET, the G_M and C_G in equation (2) are normalized by different W_G; the G_M is normalized by a smaller W_G since the transistor G_M occurs only on the 3D channels. However, the C_G builds up mostly on the channels, but also in the gaps with an overall larger W_G so f_T usually is reduced. As the 3D channels approach a corrugated mesa the f_T would approach a planar FET.

For RF applications, the maximum frequency of oscillation (f_{max}) is accepted as the best figure of merit (FoM) and incorporates device layout such as ohmic and gate resistance to amplify RF signals with higher output power [83] and wireless signals need to be amplified with a power gain. The expression for f_{max} is

$$f_{max} = \frac{f_T}{2\sqrt{G_{DS}\,(R_G + R_i + R_S) + 2\pi f_T R_G C_{gd}}} \propto \frac{G_M}{\sqrt{G_{DS} + G_M}} \quad \text{(Hz)} \tag{3}$$

and is not only dependent on f_T but also the three terminal resistances (R_G, R_S, R_D), channel charging resistance (R_i), and feedback capacitance (C_{gd}). For a 3D channel offered by nanowires with improved SCE, quantitatively, G_M and output resistance ($1/G_{DS}$) are both enhanced since gate-channel electrostatic coupling is improved. Most importantly, however, it should be noted that embedded in equation (3) is a similar expression to G_o in equation (1). The f_{max}, with its dependence on G_0, could meet and perhaps exceed today's III–V HEMTs for a given gate length with improved electrostatics of a 3D III–V HEMT channel.

However, using a conventional top-down fabrication process to realize a 3D III–V HEMT would require a wrap-style heterojunction to form a 3D quantum well after etching the channel. Normally, this requires *ex situ* epitaxial regrowth of the top barrier on top of the exposed 3D fins with possible sidewall etch damage, and regrowth-associated non-abrupt interface at the heterojunction. Because of these challenges, most reported performance is based on 'nano ribbons' with a 2D electron gas (2DEG) only at the top facet. Mechanical piezoelectric-induced polarization effects, such as with GaN, are improved, but a wrap-style gate is not as beneficial since the other gated facets would be far away from the channel [84–86]. *As a result, HEMTs with 3D III–V topologies largely remain a virgin field.*

Note that carbon-based transistors with high $f_T > 400$ GHz are impressive, but yet lacking significantly in f_{max} (record at ~30–70 GHz) and I_{ON}/I_{OFF} (<100) [87–90]. Carbon nanotubes (CNTs) are a promising scaling candidate for RF devices and several groups have successfully fabricated RF CNT transistors [88, 91, 92]. However, the issue of the bandgap being extremely sensitive to CNT diameters and chiralities has not been solved at the growth stage on-chip. Currently, CNTs are mostly selected post-growth off-chip according to bandgap and spun on as a 'film' to make devices which is unfavorable for wafer-scale RF

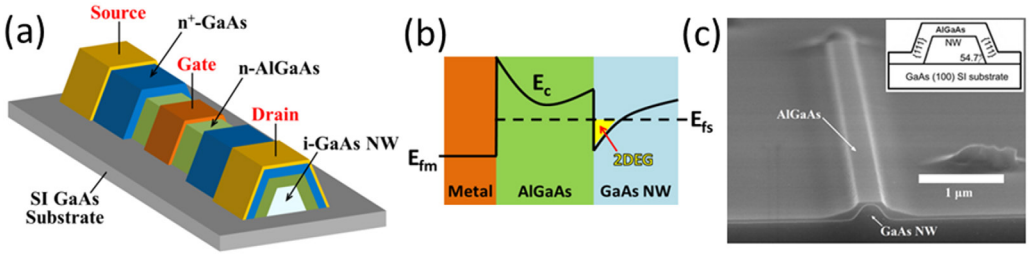

Figure 17. (a) Schematic illustration of a planar GaAs nanowire HEMT. (b) Band diagram across the gate region at the 'ON' state. (c) Tilted SEM image (focused at the front) of a cleaved sample showing the cross-section of an $Al_{0.35}Ga_{0.65}As$/GaAs-nanowire heterostructure on a SI (1 0 0) GaAs substrate. © 2011 IEEE. Reprinted, with permission, from [56].

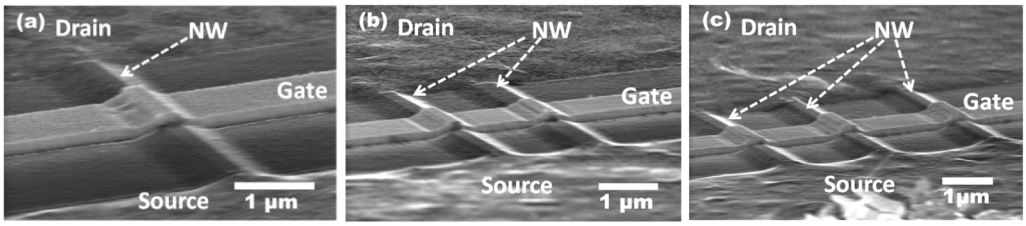

Figure 18. Long-channel planar GaAs nanowire HEMTs on a SI (1 0 0) GaAs substrate with single (a), double (b) and triple (c) planar ⟨1 1 0⟩ GaAs nanowires covered by a Si-doped $Al_{0.35}Ga_{0.65}As$ film as the channels, respectively. The three devices have the same L_g of ~1.2 μm and L_{sd} of ~5 μm. © 2011 IEEE. Reprinted, with permission, from [56].

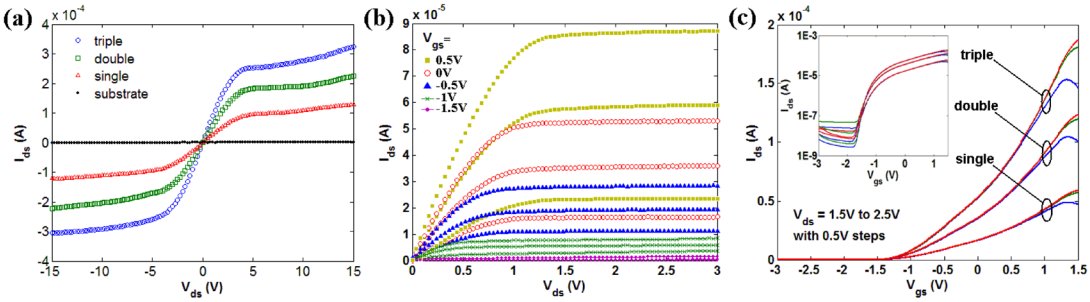

Figure 19. (a) *I–V* characteristics of two-terminal devices similar to those shown in figure 18 but without the gate electrodes. (b) Output characteristics of the devices as shown in figure 18 with V_{gs} stepped from −1.5–0.5 V. (c) Transfer characteristics of the devices as shown in figure 18 with V_{ds} stepped from 1.5 to 2.5 V. The inset is the same transfer characteristics in semi-log scale. © 2011 IEEE. Reprinted, with permission, from [56].

devices. Even with contact improvements, high-density parallel-aligned wafer-level demonstration remains a major setback for CNT-electronics. On the other hand, 2D graphene sheet has met with its zero-bandgap challenge preventing current saturation and high RF operating frequency. Other 2D crystals such as MoS_2 with a finite bandgap could emerge as a promising candidate for RF applications though it possesses lower mobility than III–V semiconductors [93, 94].

RF devices based on bottom-up growth has mainly been achieved with vertical III–V nanowires due to the out-of-plane preferential growth direction, though, at the expense of challenging fabrication. A vertical array nanowire transistor RF performance was reported by Lund University researchers demonstrating $f_T/f_{max} = 103/155$ GHz with ~32 nm diameter n-type InAs nanowires [95–97]. In a planar configuration, RF measurements have been made with single nanowire planar FETs comprised of InAs [69], AlGaN/GaN [98] and SnO_2 [99]. So far, the only reported planar array transistor is a n-type InAs nanowire-MOSFET fabricated by aligning randomly spun-on nanowires on flexible substrate but with $f_T/f_{max} < 2$ GHz [100]. Impressive III–V planar nanowires have also been formed by top-down etching but RF devices have not been fabricated [101]. Similarly, carbon-based transistors with high $f_T > 400$ GHz are impressive on one hand, but yet lacking significantly in record $f_{max} = 40$–70 GHz and $I_{ON}/I_{OFF} < 100$ [87–90].

Bottom-up grown planar III–V nanowires with inherent 3D cross-section profiles, are of particular interest because their self-assembled nature does not require extensive lithography and chemical etching to define the feature dimension and monolithic growth of the 3D channel and wrap-style barriers is feasible high frequency RF operation on a wafer-scale and highly desired. In particular, by assembling dense integrated 3D channels with negligible spacing between them, excellent DC and RF performance may be obtained. For real-world applications, RF nanoelectronics are more promising if the 3D channels are heterogeneously integrated on other platforms while reusing the III–V substrate.

5.1. Planar nanowire HEMT: DC performance

5.1.1. Long-channel planar nanowire HEMTs. It has been reported that VLS grown nanowires have non-uniform doping

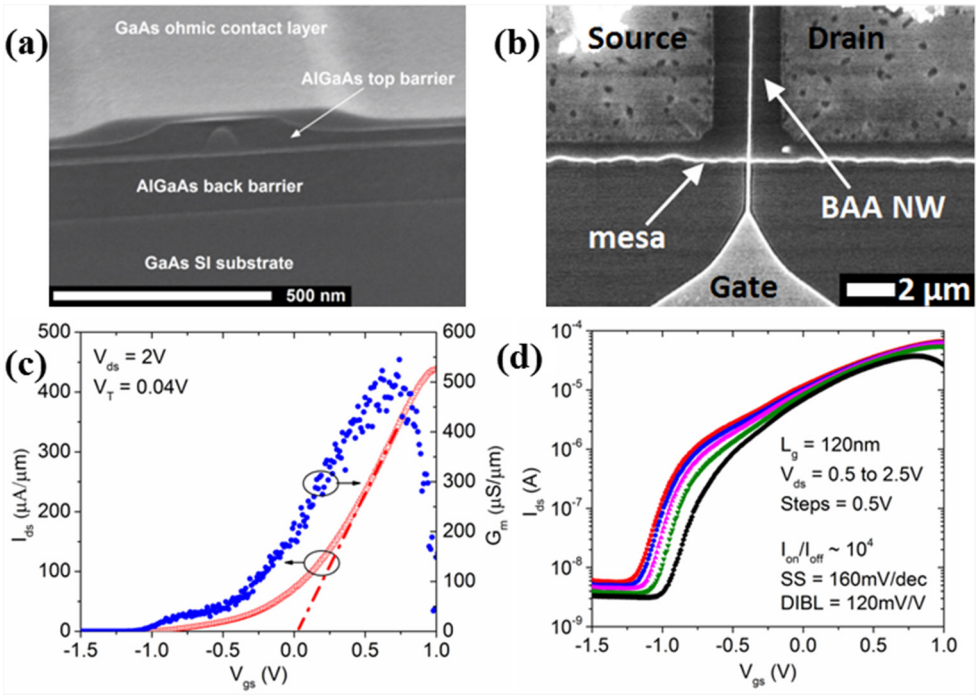

Figure 20. (a) Cross-sectional SEM image of a BAA planar GaAs nanowire heterostructure. (b) Top-view SEM image of a BAA planar GaAs nanowire HEMT with $L_g \sim 120$ nm and $L_{sd} \sim 3$ μm. (c) $I_{ds}V_{gs}$ transfer characteristics of the device as shown in (b). The peak transconductance ($G_{m\text{-}ext}$) is 550 μS μm^{-1} and the maximum drive current ($I_{d\text{-}max}$) is 435 μA μm^{-1} at $V_{ds} = 2$ V. The width normalization used $W_{eff} = 145$ nm. (d) Semi-log $I_{ds}V_{gs}$ transfer characteristics with at V_{ds} stepped from 0.5 V to 2.5 V. Reprinted with permission from [34]. Copyright 2013 American Chemical Society.

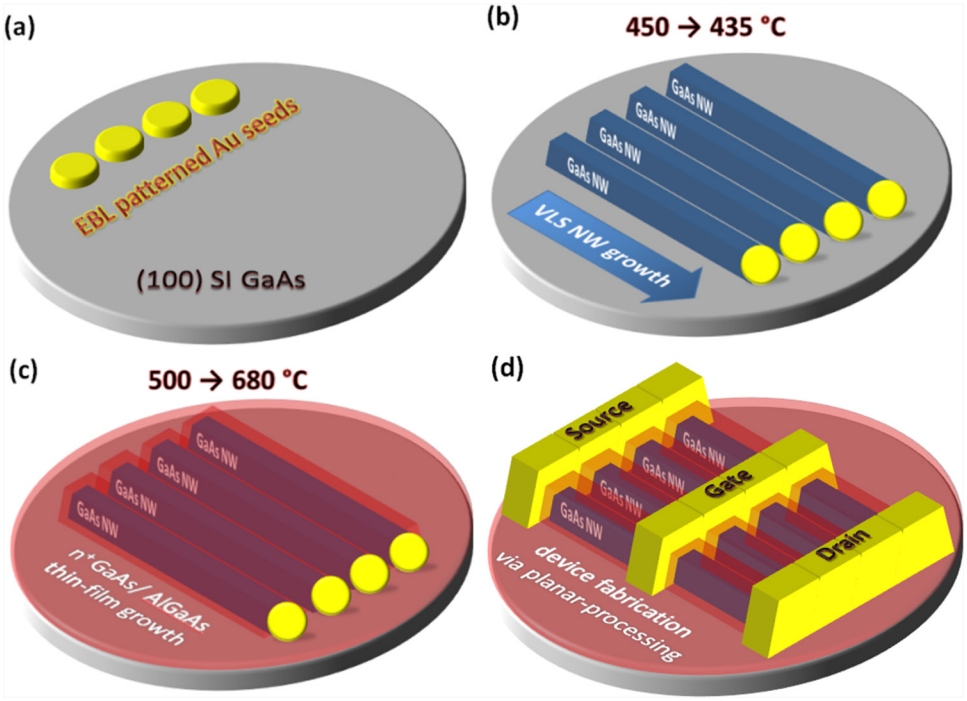

Figure 21. Illustration of the planar nanowire array-based HEMT formation process. (a) Au nanoparticles are defined by lithography followed by (b) VLS epitaxy of GaAs nanowire channels aligned by the substrate orientation. (c) Growth mode is switched to vapor solid epitaxy to form a conformal carrier supplying layer for HEMTs. (d) Metallization process, amendable to industry compatible co-planar contact geometry.

across and along the same nanowire and among different nanowires [61–63, 102, 103]. Thus, nanowire FETs using doped VLS nanowires as the channels would have inherent non-uniform electrical characteristics, which makes them not suitable for large-scale electronics applications. In order to resolve this issue, we have proposed a planar nanowire HEMT structure with intrinsic planar GaAs nanowires covered by a Si-doped AlGaAs thin film as the channel and a metal-AlGaAs Schottky junction as the gate [56]. Figures 17(a) and (b) illustrate the structure of planar GaAs nanowire

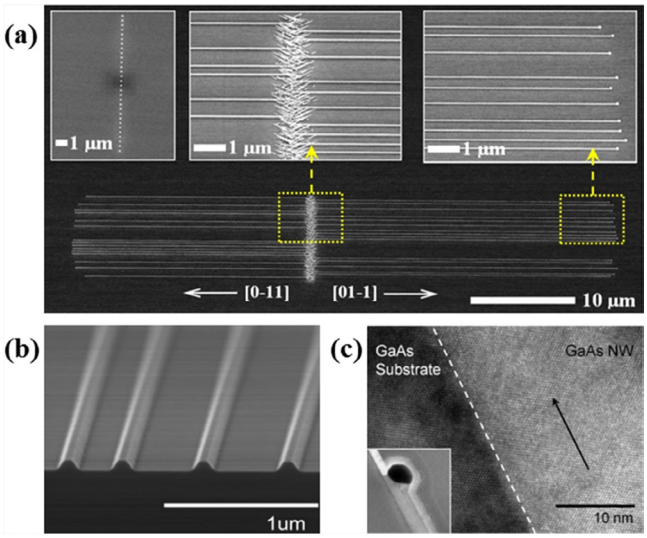

Figure 22. (a) Tilt-view SEM image of a planar ⟨1 1 0⟩ GaAs nanowire array on a SI (1 0 0) GaAs substrate with 100% planar nanowire yield. The insets, from the left to the right, show the patterned Au seeds (300 nm pitch), the dividing line between the oppositely propagated nanowires and the tips of [0 1 −1] nanowires. (b) Tilt-view SEM image of a cleaved planar GaAs nanowire array. The planar GaAs nanowires have perfectly uniform and trapezoidal cross-sections. (c) HR-TEM image of a representative planar GaAs nanowire liberated from the as-grown sample. The inset shows the cross-sectional geometry (along the nanowire) of the Au seed relative to the nanowire and substrate. Reprinted with permission from [57]. Copyright 2014 American Chemical Society.

HEMTs. Figure 17(c) is a tilt-view SEM image of a cleaved sample showing the cross-section of an $Al_{0.35}Ga_{0.65}As$/GaAs-nanowire heterostructure on a SI (1 0 0) GaAs substrate. The metal-AlGaAs Schottky gate can modulate the density of the two-dimensional electron gas (2DEG) at the AlGaAs/GaAs-nanowire interface and thus adjust the channel conductance. Because both the thickness and doping level of the AlGaAs thin film are well controllable, planar GaAs nanowire HEMTs would have uniform electrical characteristics if the nanowires have uniform sizes.

Figure 18 show three full-fabricated planar GaAs nanowire HEMTs on a SI (1 0 0) GaAs substrate with single, double and triple planar ⟨1 1 0⟩ GaAs nanowires covered by a Si-doped $Al_{0.35}Ga_{0.65}As$ film as the channels, respectively. The three devices have the same L_g of ~1.2 μm and L_{sd} of ~5 μm. Figure 19(a) plots the *I–V* characteristics of two-terminal devices similar to those shown in figure 18 but without the gate electrodes. As can be seen, the two-terminal current scales exactly with the number of nanowires between the source and drain. The *I–V* curve of a control device with no nanowire between the source and drain was also plotted for comparison, from which one can conclude that only the planar GaAs nanowires are conductive. Figures 19(b) and (c) are the output and transfer characteristics of three planar GaAs nanowire HEMTs as shown in figure 18. Apparently, the current levels of the planar GaAs nanowire HEMTs scale precisely with the number of nanowires in the channel, demonstrating that planar GaAs nanowire HEMTs have uniform and scalable electrical characteristics.

5.1.2. Short-channel planar GaAs nanowire barrier-all-around HEMTs. In order to make short-channel planar GaAs nanowire HEMTs, it is imperative to down-scale the sizes of planar GaAs nanowires to ensure good electrostatics. Adding an AlGaAs back-barrier below the planar GaAs nanowire can further enhance the electrostatics. By optimizing the growth parameters of TMGa flow, AsH_3 to TMGa molar ratio (V/III ratio) and temperature, we managed to grow high-quality planar GaAs nanowires with diameters below 50 nm and parasitic thin film to nanowire growth rate ratio lower than 0.001 [34]. We have also developed a monolithic growth method to grow barrier-all-around (BAA) planar GaAs nanowires with an intrinsic $Al_{0.33}Ga_{0.67}As$ back-barrier and a Si-doped $Al_{0.33}Ga_{0.67}As$ top-barrier below and over the nanowires through growth mode modulation by adjusting the growth temperature and reactor pressure [27, 34].

Shown in figure 20(a) is the cross-section of the BAA planar GaAs nanowire heterostructure that was used for short-channel planar GaAs nanowire HEMT fabrication. The periphery of the nanowire channel's conducting surfaces (two side-walls plus one top facet) is ~145 nm. This is also the nanowire channel's effective width (W_{eff}). Figure 20(b) shows the top-view SEM image of a BAA planar GaAs nanowire HEMT with L_g ~ 120 nm and L_{sd} ~ 3 μm. Because of the short gate length, high-quality scaled planar GaAs nanowire channel and enhanced carrier confinement from the BAA heterostructure, the device has excellent DC characteristics. Figures 20(c) and (d) are the transfer characteristics of the device in linear and semi-log scale, from which peak transconductance ($G_{m\text{-}ext}$) of 550 μS μm^{-1}, maximum drive current ($I_{d\text{-}max}$) of 435 μA μm^{-1}, I_{on}/I_{off} of 10^4, sub-threshold slope (SS) of 160 mV/dec and drain-induced-barrier-lowering (DIBL) of 120 mV V^{-1} can be extracted. The achieved $G_{m\text{-}ext}$ and $I_{d\text{-}max}$ are comparable or even better than what can be achieved from the thin-film HEMT counterparts, indicating planar GaAs nanowire HEMTs' potential for high-speed electronics application. Similar core–shell nanowire HEMTs have also been realized on vertical nanowires [104, 105]. The device with InGaAs core and multiple shells showed very high transconductance [104], which is partly due to the intrinsically high electron mobility in InGaAs.

5.1.3. Planar GaAs nanowire array-based HEMTs. The planar GaAs nanowire HEMTs discussed above were made from planar GaAs nanowires grown from dispersed Au colloids. Those planar GaAs nanowires have random positioning and broad size distribution. In order to make planar GaAs nanowires feasible for practical device applications, we developed a method (figure 21) to grow planar GaAs nanowire arrays from patterned Au seeds [35, 57] and demonstrated >100 planar GaAs nanowire array-based HEMTs on a 1.5 × 1.5 cm^2 device

Figure 22(a) is a tilt-view SEM image of a representative planar ⟨1 1 0⟩ GaAs nanowire array grown on a SI (1 0 0) GaAs substrate that would serve as the conducting channel of a HEMT. The planar GaAs nanowires grow bi-directionally

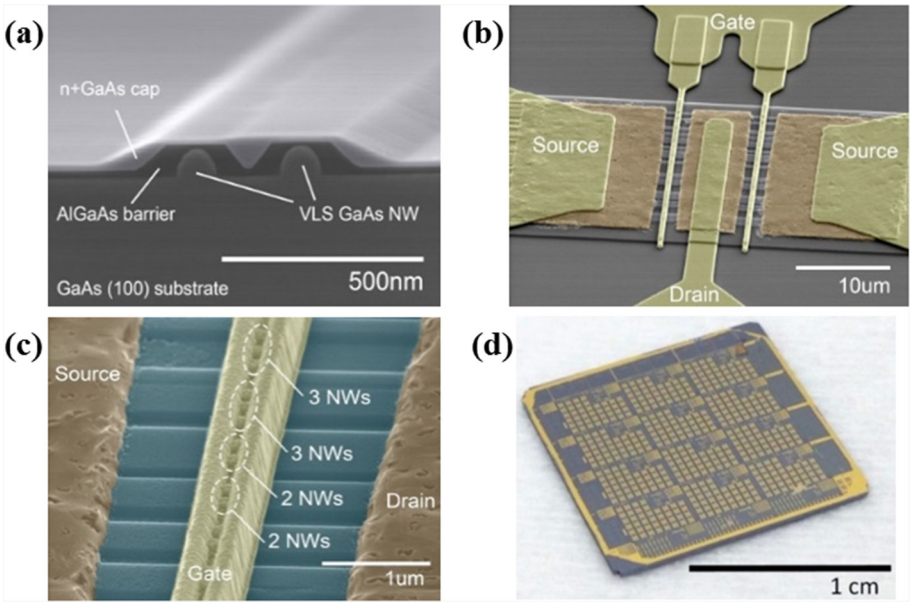

Figure 23. (a) Tilt-view SEM image of the cross-section of planar GaAs nanowire HEMT heterostructure. (b) A representative planar GaAs nanowire array-based HEMT with $L_g \sim 150$ nm and $L_{sd} \sim 3$ μm in a double-gate RF layout configuration. The double gates shared the same [0 1 −1] planar GaAs nanowire array. (c) Zoom-in image of the channel region. The morphology of the AlGaAs/GaAs-nanowire structures were revealed under the *T*-gate where the GaAs ohmic contact layer was selectively removed. (d) A $1.5 \times 1.5\,cm^2$ device chip consisting >100 precisely positioned planar GaAs nanowire array-based HEMTs as shown in (b). Reprinted with permission from [57] Copyright 2014 American Chemical Society.

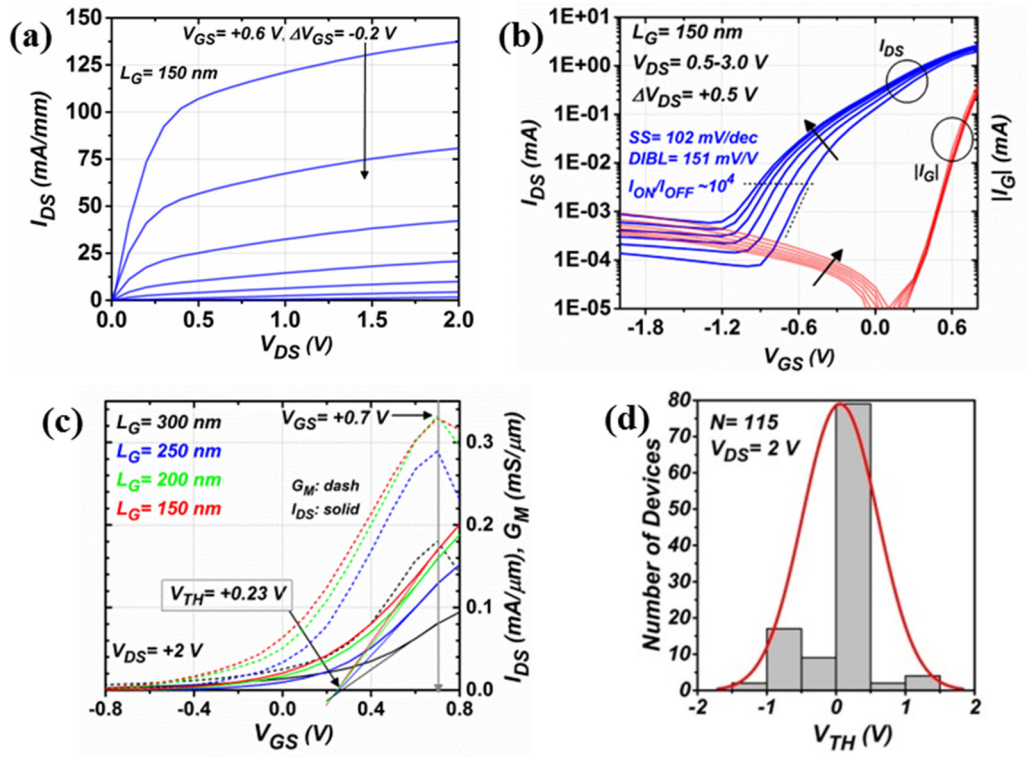

Figure 24. DC characteristics of planar GaAs nanowire array-based HEMTs. (a) Output characteristics of the device ($L_g \sim 150$ nm) shown in figure 23(b). (b) Transfer characteristics of the device ($L_g \sim 150$ nm) shown in figure 23(b). (c) Transfer characteristics of four devices with different gate lengths. (d) V_t distribution of all 115 devices on the device chip. Reprinted with permission from [57]. Copyright 2014 American Chemical Society.

in the anti-parallel [0 −1 1] (towards the left) and [0 1 −1] (towards the right) directions. The insets of figure 22(a), from the left to the right, show the patterned Au seeds (300 nm pitch), the dividing line between the oppositely propagated nanowires and the tips of the [0 1 −1] nanowires. As can be seen, the planar GaAs nanowires and the patterned Au seeds have one-to-one correspondence. The tilt-view SEM image of a cleaved planar GaAs nanowire array is shown in figure 22(b).

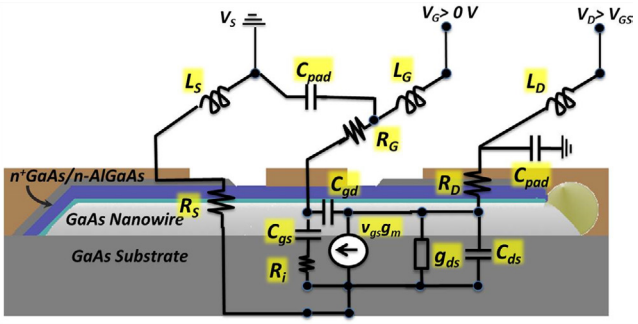

Figure 25. Conventional HEMT small-signal model with extrinsic and intrinsic passive elements (see text for details) superimposed on a nanowire-HEMT. Reproduced from [51]. © IOP Publishing Ltd. All rights reserved.

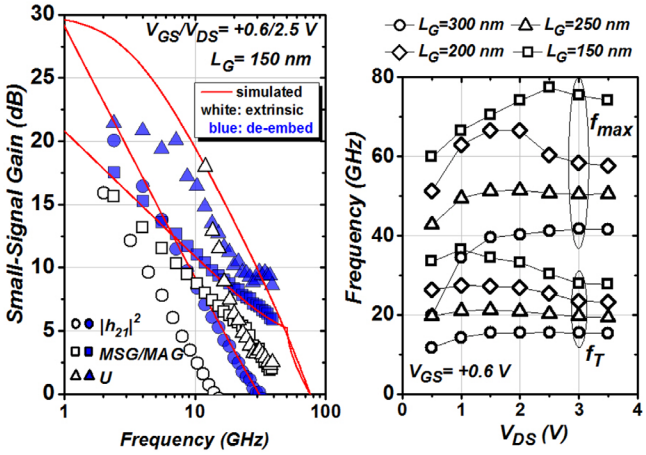

Figure 26. (Left) Representative simulated (red line), extrinsic (clear symbol) and de-embedded (blue symbol) f_T and f_{max} at $V_{GS}/V_{DS} = +0.6/2.5$ V for $L_G = 150$ nm. (Right) De-embedded f_T, f_{max} versus V_{GS}, V_{DS} for $L_G = 300$ nm, 250 nm, 200 nm, 150 nm at the G_M peak gate bias [57, 58]. © 2015 IEEE. Reprinted, with permission, from [57, 58].

The planar GaAs nanowires have a trapezoidal cross-section and perfectly uniform dimensions. High-resolution transmission electron microscopy (HR-TEM) analysis was done on a representative planar GaAs nanowire liberated from the as-grown sample, which revealed that the planar ⟨1 1 0⟩ GaAs nanowire has a purely zinc-blende crystal structure, and is entirely free of twin-defects and stacking faults. Figure 22(c) shows the HR-TEM image with the black arrow indicating the nanowire growth direction, and the inset shows the cross-sectional geometry (along the nanowire) of the Au seed relative to the nanowire and substrate.

Figure 23(a) shows the AlGaAs/GaAs-nanowire heterostructure used for planar GaAs nanowire array-based HEMTs fabrication. The thin-film stack over the nanowires includes a 3 nm undoped $Al_{0.33}Ga_{0.67}As$ spacer layer, a ~50 nm Si-doped ($3 \cdot 10^{18}$ cm^{-3}) $Al_{0.33}Ga_{0.67}As$ barrier layer and a Si-doped ($5 \cdot 10^{18}$ cm^{-3}) GaAs ohmic contact layer. Figure 23(b) is a representative planar GaAs nanowire array-based HEMT with L_g ~ 150 nm and L_{sd} ~ 3 μm in a double-gate RF layout configuration. The double gates shared the same [0 1 −1] planar GaAs nanowire array. Figure 23(c) is a zoom-in image of the channel region showing the morphology of the AlGaAs/GaAs-nanowire structures under the *T*-gate where the GaAs ohmic contact layer was selectively removed. Figure 23(d) shows the 1.5 × 1.5 cm^2 device chip consisting of >100 precisely positioned planar GaAs nanowire array-based HEMTs as shown in figure 23(b).

The DC characteristics of the planar GaAs nanowire array-based HEMTs are shown in figure 24. The gated width of each planar GaAs nanowire is ~210 nm (two side-walls plus one top facet), and the W_{eff} of a device is the total gated width of all nanowires in the channel. Figures 24(a) and (b) are the output and transfer *I–V* curves of the device (L_g ~ 150 nm) shown in figure 23(b) from which I_{on}/I_{off} of 10^4, SS of 102 mV/dec and DIBL of 151 mV V^{-1} were extracted. Figure 24(c) shows the transfer characteristics of four devices with different gate lengths. As can be seen, the four devices have nearly the same V_t and the same gate bias at the peak $G_{m\text{-}ext}$. Figure 24(d) plots the V_t of all 115 devices on the device chip, indicating uniform electrical characteristics over the entire chip. The outliers in figure 24(d) are due to un-optimized gate recess etching which can be further improved.

5.2. Planar GaAs nanowire HEMTs: RF performance and modeling

Small-signal RF performance was characterized in the 0.1–40 GHz range for each L_G for the nanowire-HEMT device and small-signal model was established to extract intrinsic values. Figure 25 shows a typical SSM superimposed on the 3D channel to understand the limiting and contributing factors for high-speed performance. The intrinsic transistor region consists of intrinsic terminal capacitance (C_{gs},C_{gd},C_{ds}), current source ($v_{gs}{}^* g_{mi}$ where g_{mi} is the intrinsic transconductance) and output conductance (g_{ds}). An added term, R_i, is the intrinsic resistance associated with the charging time of the gate capacitance. The extrinsic components are represented by inductance (L_S, L_D, L_G), resistance (R_S, R_D, R_G) and pad layout capacitance (C_{pg},C_{pd}).

To simplify the SSM equivalent circuit to solve for the various elements, the transistor is biased in the off-state, zero-bias state and on-state [106, 107]. Representative gain versus frequency and L_G measurements are shown in figure 26 at $V_{GS}/V_{DS} = +0.6/2.0$ V with the typical inverse L_G frequency scaling being observed. As expected, the power gain was much higher than the current gain which is likely due to increased gate capacitance but improved G_0 and low *T*-gate resistance.

The best de-embedded frequency performance, f_T/f_{max} ~ 33/75 GHz, was from the device with $L_G = 150$ nm measured at $V_{DS} = 2$ V, where the feedback capacitance (C_{gd}) is the least for high f_{max}. To our knowledge, this is the highest reported f_{max} achieved on any nanoscale device with VLS nanowires, CNTs or 2D sheets aligned in-plane with the substrate [87–90, 100]. The contour plots of de-embedded f_T and f_{MAX} for all four devices with $L_G = 150$, 200, 250, and 300 nm, are shown in figure 27.

While many extraction techniques exist in literature, a simple least squares fitting routine is sufficient to understand limiting and contributing factors on the RF performance of a nanowire-HEMT [108]. The resulting measured and simulated *S*-parameters are plotted in figure 28 (left) displaying excellent agreement. We now extract the intrinsic gain of the $L_G = 150$ nm nanowire-HEMT device. The L_G-independent $C_{g,e}$ can be

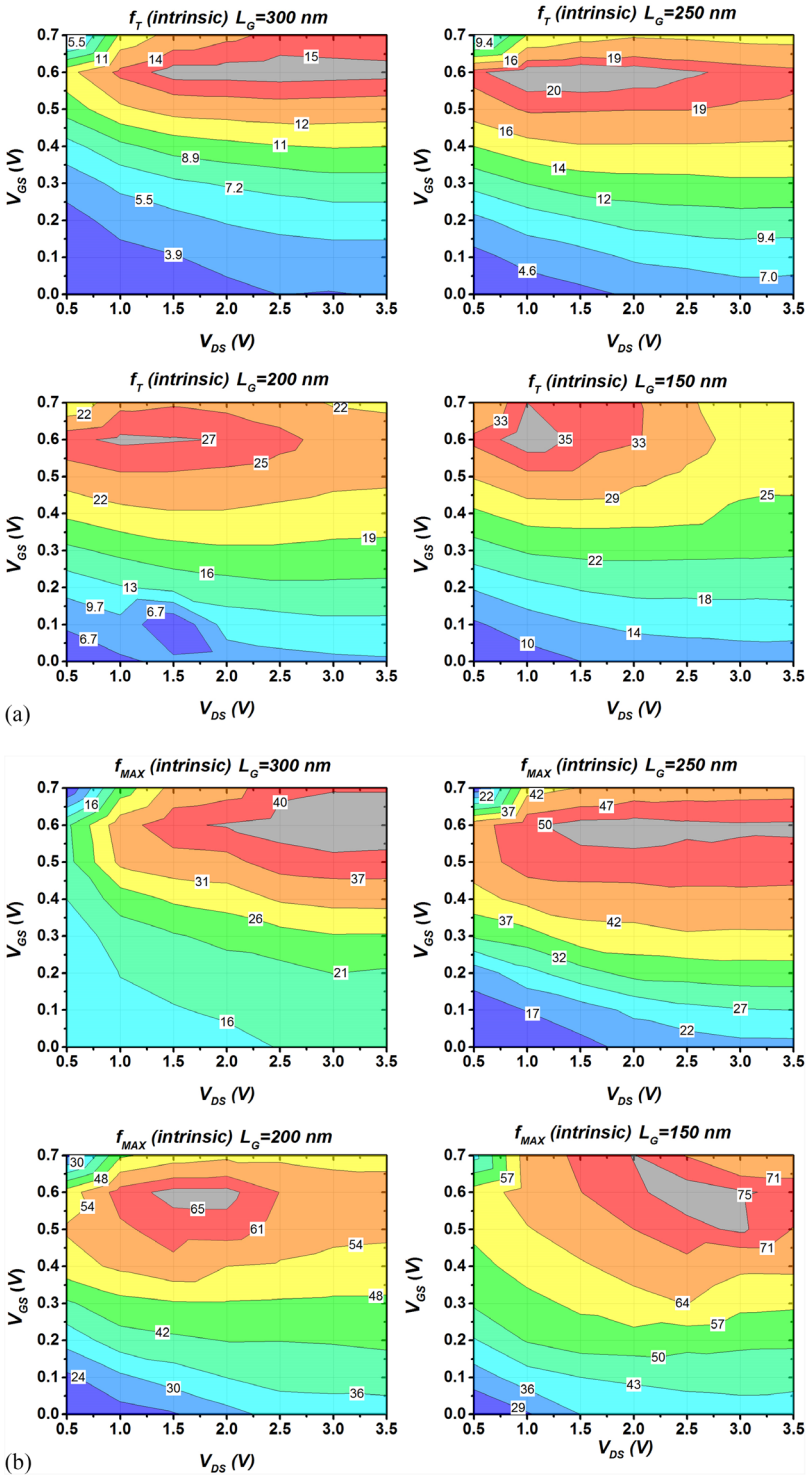

Figure 27. De-embedded (a) f_T and (b) f_{max} contour plots versus V_{GS}, V_{DS} for $L_G = 300\,nm$, $250\,nm$, $200\,nm$, $150\,nm$. © 2015 IEEE. Reprinted, with permission, from [57, 58].

extracted from the intercept of a C_g versus L_G plot in figure 28 (right). For each gated device, the C_g is normalized by taking the three-sided gated perimeter of each nanowire multiplied by the number of nanowires. $C_{gs,e}$ and $C_{gd,e}$ were found to be 15.8 fF and 6.8 fF, respectively. The slope of C_{gs} and C_{gd} versus L_G defines the L_G-dependent elements, $C_{gs,i}$ and $C_{gd,i}$, which are 7.5 fF and 3.5 fF, respectively. When comparing these values to the total extracted C_{gs} and C_{gd}, we find $C_{gs,i}/C_{gs}$ and $C_{gd,i}/C_{gd}$ are 33% and 35%, respectively. In other words, ~2/3 of the total extracted C_g is parasitic. Most of $C_{g,p}$ is likely caused by the bi-directional VLS nanowire growth which can be optimized on (1 1 0) GaAs substrate orientation for unidirectional nanowire assembly and immediately enhance the g_m/C_g ratio for higher f_T/f_{max} [36]. The total intrinsic delay, τ_i, is expressed as $C_{gs,i}/g_{mi}$ which is approximately 1.86 ps for the nanowire-HEMT device with $L_G = 150\,nm$. Removing the fringing capacitance, a theoretical f_T can be determined by equation (2) which is ~85 GHz. A theoretical ideal f_{max} can be calculated from

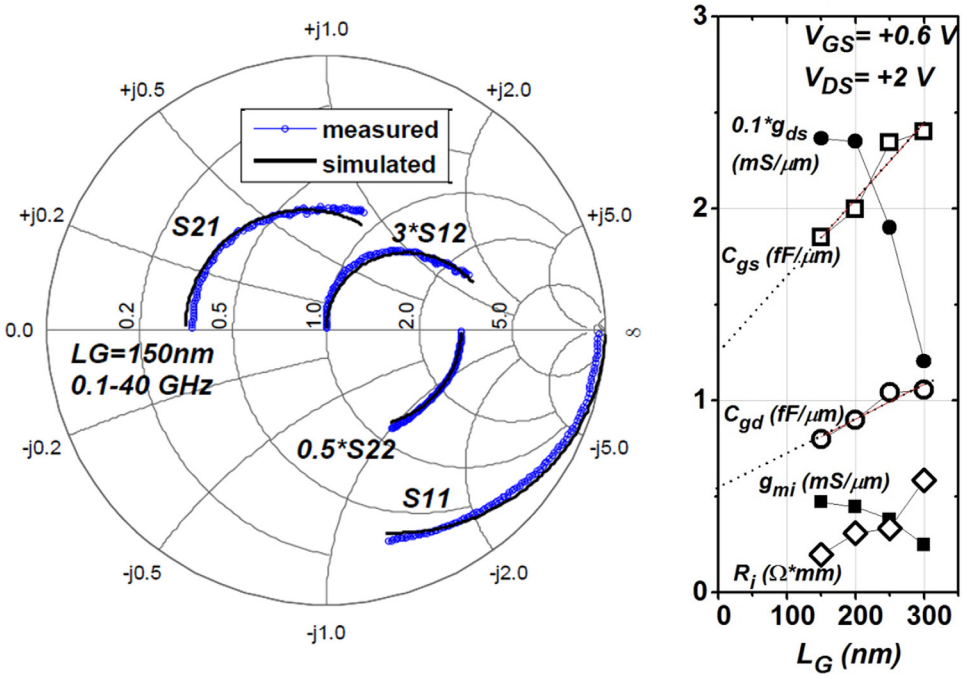

Figure 28. (Left) Smith chart illustrating excellent agreement between measured and simulated *S*-parameters for a planar GaAs/AlGaAs nanowire HEMT device with $L_G = 150$ nm at $V_{GS} = 0.6$ and $V_{DS} = 2$ V. (Right) Extracted SSM parameters (C_{gs}, C_{gd}, g_{ds}, g_{mi}, R_i) for high f_{max}, normalized for the total nanowire width, as a function of L_G; the fitting lines for C_{gs} and C_{gd} are also shown. © 2015 IEEE. Reprinted, with permission, from [58].

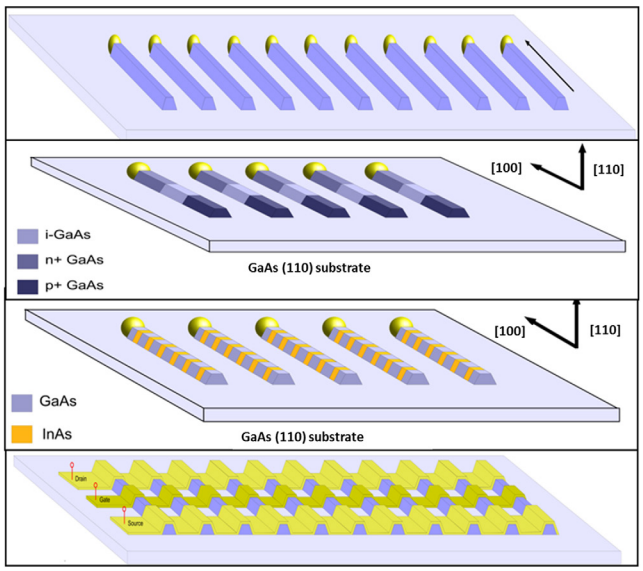

Figure 29. Illustration of planar nanowire arrays (a) that are perfectly parallel and high density with inherent 3D cross-section, (b) with lateral p–i–n junctions, (c) with lateral heterojunctions, (d) with planar processing compatible metal contacts formed. GaAs (1 1 0) substrate is used as an example.

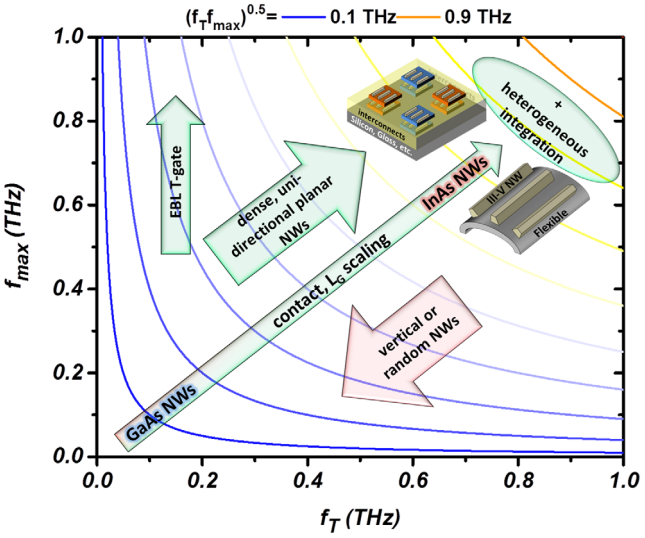

Figure 30. Schematic illustration of the envisioned paths for nanowire HEMT to reach THz operation, including changing GaAs nanowires to higher mobility InAs nanowires while scaling L_G, reducing contact resistance, increasing the planar unidirectional nanowire density (not vertical or randomly assembled nanowires) as well as vertical stacking and heterogenous integration on flexible substrates.

$$f_{max} = \sqrt{\frac{f_T}{8\pi R_G C_{gd,i}}} \quad \text{(Hz)} \tag{4}$$

and is approximately 248 GHz. Both of these theoretical values represent the upper limits of the nanowire-HEMT using GaAs/AlGaAs as the channel material and are difficult to achieve without extreme optimization of the nanowire assembly and device contacts. Despite this, the reported extrinsic $f_{max} = 78$ GHz is highest compared to other VLS nanowire FETs with planar nanowires along the substrate surface. The high f_{max} is attributed to low device resistance and good intrinsic gain. High $C_{g,p}$ limiting RF performance can be improved with device engineering and unidirectional planar VLS nanowire growth on future samples.

7. Conclusion and outlook

The planar nanowire growth approach via selective lateral epitaxy defies the commonly perceived non-compatibility of self-assembled nanowires with existing microelectronics industry, and is extremely promising to transform self-assembled nanowire based engineering concepts to a practical solution for an important field of electronics.

On the fundamental side, this unique crystal growth paradigm is based on the popular VLS mechanism with Au nanoparticles defining the site of nanowire growth, but promoted by the strong adhesion with the substrate under appropriate growth condition to propagate in plane, while the Au seed nanoparticle stays at the growth front. Unlike traditional crystal growth where materials are added from the substrate up, planar nanowire selective lateral epitaxy grows from left to right or right to left in plane. The propagation direction is the in-plane projection of ⟨1 1 1⟩B, i.e. two equivalent directions for (1 0 0) and a single available direction for (1 1 0) substrates, as described before. Note that for III–V nanowire heterogeneous growth on Si (1 0 0) or (1 1 0) substrates (not reported here), we expect growth propagates in the four equivalent ⟨1 1 1⟩ in-plane projection directions, because there is no distinction of A and B face as in compound semiconductors. Lateral epitaxy allows the formation of lateral p–n junctions and lateral heterojunctions simply by switching the precursors in the gas phase (figure 29).

On the application side, the in-plane configuration has undoubtedly made the nanowire metal contact formation simple and compatible with planar processing. In addition, selective lateral sequential propagation of growth provides unprecedented control of structure variation in plane monolithically. Well-controlled lateral p–n junction planar nanowires have been achieved and reported separately [109–111]. Lateral heterojunctions are not as straightforward because of the solubility difference of different materials in the seed particle. The ease of switching of growth modes from lateral growth via the VLS mode to conventional thin-film deposition from substrate up via the vapor solid mode, allows high quality radial junctions such as the high performance 3D HEMT structures demonstrated here. The successful demonstration and analysis of nanowire array based high performance transistors has provided clear evidence that bottom-up grown nanowire array can be a potential candidate for high-speed low power applications.

The ultimate goal of nanowire based transistors is to make high-performance nanoscale III–V devices on virtually any insulating substrate, both rigid and flexible; thus demonstrating high level of heterogeneous integration beyond today's electronics. Specifically, developing wafer-scale, massively parallel, bottom-up grown, monolithic III–V (GaAs, InGaAs, and InAs) in-plane nanowire array-based HEMTs, for high frequency and low power RF applications, including heterogeneous integration for system-on-chip portable and wearable devices. By exploiting the inherent properties of the 3D nanowire channels, coupled with aggressive scaling, the reduction of parasitic elements, and channel engineering, high frequency (f_{max}) performance meeting or exceeding conventional HEMTs with high level of nanoscale integration can be achieved. This envisioned path for scaling in both materials and structures and anticipated performance is illustrated in figure 30. Close to THz operation on arbitrary substrates is feasible, based on quantitative estimation from the SSM discussed above, if high mobility channel material such as InAs, unidirectional dense array of nanowires, aggressively scaling with minimum parasitic capacitance and resistance can be realized.

Looking beyond the applications for nanoelectronics discussed above, the planar nanowire platform and innovative crystal growth modes can also be used for many other types of devices for size scaling and performance enhancement, including lateral tunnel junction field-effect transistors, solar cells, detectors, thermal electrics, LEDs, lasers, as well as chemical and bio medical sensing. The perfect alignment this platform enables with extremely high density packing of nanowires limited only by lithography patterning of the catalyst nanoparticles, should continue to help accelerate the advancement of fundamental nano concepts into engineering solutions.

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References

[1] del Alamo J A 2011 Nanometre-scale electronics with III–V compound semiconductors *Nature* **479** 317–23
[2] Chau R, Datta S and Majumdar A 2005 Opportunities and challenges of III–V nanoelectronics for future high-speed, low-power logic applications *Compound Semiconductor Integrated Circuit Symp.* pp 17–20
[3] Reuss R H *et al* 2005 Macroelectronics: perspectives on technology and applications *Proc. IEEE* **93** 1239–56
[4] Wagner R S and Ellis W C 1964 Vapor–liquid–solid mechanism of single crystal growth *Appl. Phys. Lett.* **4** 89
[5] Redwing J M, Miao X and Li X 2014 Vapor–liquid–solid growth of semiconductor nanowires *Handbook of Crystal Growth: Thin Films and Epitaxy* 2nd edn (Amsterdam: Elsevier) pp 399–439
[6] Persson A I *et al* 2004 Solid-phase diffusion mechanism for GaAs nanowire growth *Nat. Mater.* **3** 677
[7] Dick K A *et al* 2005 Failure of the vapor–liquid–solid mechanism in au-assisted MOVPE growth of InAs nanowires *Nano Lett.* **5** 761–4
[8] Gao L *et al* 2009 Self-catalyzed epitaxial growth of vertical indium phosphide nanowires on silicon *Nano Lett.* **9** 3379
[9] Wu Z H *et al* 2003 Growth, branching, and kinking of molecular-beam epitaxial ⟨1 1 0⟩ GaAs nanowires *Appl. Phys. Lett.* **83** 3368–70
[10] Wang N, Cai Y and Zhang R Q 2008 Growth of nanowires *Mater. Sci. Eng.* R **60** 1–51
[11] Kim B J *et al* 2008 Kinetics of individual nucleation events observed in nanoscale vapor–liquid–solid growth *Science* **322** 1070–3
[12] Hiruma K *et al* 1995 Growth and optical properties of nanometer-scale GaAs and InAs whiskers *J. Appl. Phys.* **77** 447–62

[13] Agarwal R and Lieber C M 2006 Semiconductor nanowires: optics and optoelectronics *Appl. Phys.* A **85** 209–15
[14] Li Y *et al* 2006 Nanowire electronic and optoelectronic devices *Mater. Today* **9** 18–27
[15] Samuelson L *et al* 2004 Semiconductor nanowires for 0D and 1D physics and applications *Physica* E **25** 313–8
[16] Pearton S J *et al* 2008 GaN, ZnO and InN nanowires and devices *J. Nanosci. Nanotechnol.* **8** 99–110
[17] Lu W and Lieber C M 2007 Nanoelectronics from the bottom up *Nat. Mater.* **6** 841–50
[18] Blanchard P T *et al* 2008 MESFETs made from individual GaN nanowires *IEEE Trans. Nanotechnol.* **7** 760–5
[19] Dayeh S A *et al* 2008 Field dependent transport properties in InAs nanowire field effect transistors *Nano Lett.* **8** 3114–9
[20] Huang Y *et al* 2001 Directed assembly of one-dimensional nanostructures into functional networks *Science* **291** 630–3
[21] Yu G H, Cao A Y and Lieber C M 2007 Large-area blown bubble films of aligned nanowires and carbon nanotubes *Nat. Nanotechnol.* **2** 372–7
[22] Fan Z Y *et al* 2008 Wafer-scale assembly of highly ordered semiconductor nanowire arrays by contact printing *Nano Lett.* **8** 20–5
[23] Fan D L, Cammarata R C and Chien C L 2008 Precision transport and assembling of nanowires in suspension by electric fields *Appl. Phys. Lett.* **92** 093115
[24] Pauzauskie P J *et al* 2006 Optical trapping and integration of semiconductor nanowire assemblies in water *Nat. Mater.* **5** 97–101
[25] Fortuna S A and Li X 2010 Metal-catalyzed semiconductor nanowires: a review on the control of growth directions *Semicond. Sci. Technol.* **25** 024005
[26] Haraguchi K *et al* 1996 Self-organized fabrication of planar GaAs nanowhisker arrays *Appl. Phys. Lett.* **69** 386–7
[27] Fortuna S A *et al* 2008 Planar GaAs nanowires on GaAs (1 0 0) substrates: self-aligned, nearly twin-defect free, and transfer-printable *Nano Lett.* **8** 4421–7
[28] Zota C B, Wernersson L-E and Lind E 2014 $In_{0.53}Ga_{0.47}As$ multiple-gate field-effect transistors with selectively regrown channels *IEEE Electron Device Lett.* **35** 342–4
[29] Zota C B *et al* 2014 Radio-frequency characterization of selectively regrown InGaAs lateral nanowire MOSFETs *IEEE Trans. Electron Devices* **61** 4078–83
[30] Coleman J J *et al* 1997 Progress in InGaAs-GaAs selective-area MOCVD toward photonic integrated circuits *IEEE J. Sel. Top. Quantum Electron.* **3** 874–84
[31] Akabori M, Murakami T and Yamada S 2012 Selective area molecular beam epitaxy of InAs on GaAs (1 1 0) masked substrates for direct fabrication of planar nanowire field-effect transistors *J. Cryst. Growth* **345** 22–6
[32] Schmid H *et al* 2015 Template-assisted selective epitaxy of III–V nanoscale devices for co-planar heterogeneous integration with Si *Appl. Phys. Lett.* **106** 233101
[33] Dowdy R *et al* 2012 Realization of unidirectional planar GaAs nanowires on GaAs (1 1 0) substrates *IEEE Electron Device Lett.* **33** 522–4
[34] Miao X, Zhang C and Li X 2013 Monolithic barrier-all-around high electron mobility transistor with planar GaAs nanowire channel *Nano Lett.* **13** 2548–52
[35] Zhang C *et al* 2014 Site-controlled VLS growth of planar nanowires: yield and mechanism *Nano Lett.* **14** 6836–41
[36] Dowdy R S, Walko D A and Li X 2013 Relationship between planar GaAs nanowire growth direction and substrate orientation *Nanotechnology* **24** 035304
[37] Zhang G *et al* 2010 Parallel-aligned GaAs nanowires with 110 orientation laterally grown on [3 1 1]B substrates via the gold-catalyzed vapor–liquid–solid mode *Nanotechnology* **21** 095607
[38] Givargizov E I 1975 Fundamental aspects of VLS growth *J. Cryst. Growth* **31** 20–30
[39] Chau R *et al* 2005 Benchmarking nanotechnology for high-performance and low-power logic transistor applications *IEEE Trans. Nanotechnol.* **4** 153–8
[40] Chang S W *et al* 2013 InAs N-MOSFETs with record performance of $I_{on} = 600$ μA μm^{-1} at $I_{off} = 100$ nA μm^{-1} ($V_d = 0.5$ V) *IEEE Int. Electron Device Meeting (IEDM)* pp 16.1.1–4
[41] Czornomaz L *et al* 2013 Co-integration of InGaAs n- and SiGe p-MOSFETs into digital CMOS circuits using hybrid dual-channel ETXOI substrates *IEEE Int. Electron Devices Meeting (IEDM)* (https://doi.org/10.1109/IEDM.2013.6724548)
[42] Zhang C and Li X 2016 III–V nanowire transistors for low-power logic applications: a review and outlook *IEEE Trans. Electron Devices* **63** 223–34
[43] People R and Bean J C 1985 Calculation of critical layer thickness versus lattice mismatch for Ge_xSi_{1-x}/Si strained-layer heterostructures *Appl. Phys. Lett.* **47** 322
[44] Sasaki A 1996 Initial growth layers and critical thickness of InAs heteroepitaxy on GaAs substrates *J. Cryst. Growth* **160** 27–35
[45] Matthews J W and Blakeslee A E 1974 Defects in epitaxial multilayers: I. Misfit dislocations *J. Cryst. Growth* **27** 118–25
[46] Houzay F *et al* 1987 First stages of the MBE growth of InAs on (0 0 1)GaAs *J. Cryst. Growth* **81** 67–72
[47] Moison J M *et al* 1994 Self-organized growth of regular nanometer-scale InAs dots on GaAs *Appl. Phys. Lett.* **64** 196
[48] Munekata H *et al* 1987 Lattice relaxation of InAs heteroepitaxy on GaAs *J. Cryst. Growth* **81** 237–42
[49] Nabetani Y *et al* 1995 Island formation of InAs grown on GaAs *J. Cryst. Growth* **146** 363–7
[50] Chuang L C *et al* 2007 Critical diameter for III–V nanowires grown on lattice-mismatched substrates *Appl. Phys. Lett.* **90** 043115
[51] Ghalamestani S G *et al* 2012 Uniform and position-controlled InAs nanowires on 2″ Si substrates for transistor applications *Nanotechnology* **23** 015302
[52] Yamaguchi M *et al* 2011 In-assisted catalyst-free MBE-VLS growth of InAs nanowires on Si substrate *AIP Conf. Proc.* **1399** 229–30
[53] Tomioka K *et al* 2008 Control of InAs nanowire growth directions on Si *Nano Lett.* **8** 3475–80
[54] Hertenberger S *et al* 2010 Growth kinetics in position-controlled and catalyst-free InAs nanowire arrays on Si(1 1 1) grown by selective area molecular beam epitaxy *J. Appl. Phys.* **108** 114316
[55] Gomes U P *et al* 2015 Catalyst-free growth of InAs nanowires on Si (1 1 1) by CBE *Nanotechnology* **26** 415604
[56] Miao X and Li X 2011 Scalable monolithically grown AlGaAs–GaAs planar nanowire high-electron-mobility transistor *IEEE Electron Device Lett.* **32** 1227–9
[57] Miao X *et al* 2014 High-speed planar GaAs nanowire arrays with $f_{max} > 75$ GHz by wafer-scale bottom-up growth *Nano Lett.* **15** 2780–6
[58] Chabak K D *et al* 2015 RF performance of planar III–V nanowire-array transistors grown by vapor–liquid–solid epitaxy *IEEE Electron Device Lett.* **36** 445–7
[59] Sun Y *et al* 2006 Buckled and wavy ribbons of GaAs for high-performance electronics on elastomeric substrates *Adv. Mater.* **18** 2857–62
[60] Fortuna S A and Li X 2009 GaAs MESFET with a high-mobility self-assembled planar nanowire channel *IEEE Electron Device Lett.* **30** 593–5
[61] Schwalbach E and Voorhees P 2009 Doping nanowires grown by the vapor–liquid–solid mechanism *Appl. Phys. Lett.* **95** 063105
[62] Perea D E *et al* 2009 Direct measurement of dopant distribution in an individual vapour–liquid–solid nanowire *Nat. Nanotechnol.* **4** 315–9

[63] Gutsche C *et al* 2009 Controllable p-type doping of GaAs nanowires during vapor–liquid–solid growth *J. Appl. Phys.* **105** 4305

[64] Sotoodeh M, Khalid A and Rezazadeh A 2000 Empirical low-field mobility model for III–V compounds applicable in device simulation codes *J. Appl. Phys.* **87** 2890–900

[65] Zhang C, Dowdy R and Li X 2013 High voltage gain MESFET amplifier using self-aligned MOCVD grown planar GaAs nanowires *Device Research Conf. (DRC)* pp 63–4

[66] Zhang C and Li X 2014 Planar GaAs nanowire tri-gate MOSFETs by vapor–liquid–solid growth *Solid-State Electron.* **93** 40–42

[67] Zhang C *et al* 2015 InAs planar nanowire gate-all-around MOSFETs on GaAs substrates by selective lateral epitaxy *IEEE Electron Device Lett.* **36** 663–5

[68] Zhang C *et al* 2015 InAs nanowire gate-all-around MOSFETs by heterogeneous planar VLS growth *Device Research Conf. (DRC), 2015 73rd Annual* (https://doi.org/10.1109/DRC.2015.7175616)

[69] Blekker K *et al* 2010 High-frequency measurements on InAs nanowire field-effect transistors using coplanar waveguide contacts *IEEE Trans. Nanotechnol.* **9** 432–7

[70] Chen S Y *et al* 2013 Influence of catalyst choices on transport behaviors of InAs NWs for high-performance nanoscale transistors *Phys. Chem. Chem. Phys.* **15** 2654–9

[71] Dey A W *et al* 2012 High-performance InAs nanowire MOSFETs *IEEE Electron Device Lett.* **33** 791–3

[72] Ford A C *et al* 2009 Diameter-dependent electron mobility of InAs nanowires *Nano Lett.* **9** 360–5

[73] Jiang X *et al* 2007 InAs/InP radial nanowire heterostructures as high electron mobility devices *Nano Lett.* **7** 3214–8

[74] Vasen T *et al* 2016 InAs nanowire GAA n-MOSFETs with 12–15 nm diameter *2016 IEEE Symp. on VLSI Technology* pp 1–2

[75] Dayeh S A *et al* 2007 High electron mobility InAs nanowire field-effect transistors *Small* **3** 326–32

[76] Persson K-M *et al* 2012 Vertical InAs nanowire MOSFETs with $I_D = 1.34$ mA μm^{-1} and $g_m = 1.19$ mS μm^{-1} at $V_D = 0.5$ V *Device Research Conf.* pp 195–6

[77] Rehnstedt C *et al* 2008 Vertical InAs nanowire wrap gate transistors on Si substrates *IEEE Trans. Electron Devices* **55** 3037–41

[78] Tanaka T *et al* 2010 Vertical surrounding gate transistors using single InAs nanowires grown on Si substrates *Appl. Phys. Express* **3** 025003

[79] Thelander C *et al* 2008 Development of a vertical wrap-gated InAs FET *IEEE Trans. Electron Devices* **55** 3030–6

[80] Bryllert T *et al* 2006 Vertical high-mobility wrap-gated InAs nanowire transistor *IEEE Electron Device Lett.* **27** 323–5

[81] Lin J *et al* 2014 A novel digital Etch technique for deeply scaled III–V MOSFETs *IEEE Electron Device Lett.* **35** 440–2

[82] Taur Y and Ning T H 2013 *Fundamentals of Modern VLSI Devices* (Cambridge: Cambridge University Press)

[83] Schwierz F and Liou J J 2001 Semiconductor devices for RF applications: evolution and current status *Microelectron. Reliab.* **41** 145–68

[84] Zimmermann T *et al* 2009 Top-down AlN/GaN enhancement and depletion-mode nanoribbon HEMTs *Device Research Conf., DRC 2009* (https://doi.org/10.1109/DRC.2009.5354874)

[85] Azize M *et al* 2011 High-electron-mobility transistors based on InAlN/GaN nanoribbons *IEEE Electron Device Lett.* **32** 1680–2

[86] Azize M and Palacios T 2011 Top-down fabrication of AlGaN/GaN nanoribbons *Appl. Phys. Lett.* **98** 042103

[87] Wu Y *et al* 2012 State-of-the-art graphene high-frequency electronics *Nano Lett.* **12** 3062–7

[88] Steiner M *et al* 2012 High-frequency performance of scaled carbon nanotube array field-effect transistors *Appl. Phys. Lett.* **101** 053123–4

[89] Guo Z *et al* 2013 Record maximum oscillation frequency in C-face epitaxial graphene transistors *Nano Lett.* **13** 942–7

[90] Che Y *et al* 2013 T-gate aligned nanotube radio frequency transistors and circuits with superior performance *ACS Nano* **7** 4343–50

[91] Schroter M *et al* 2013 Carbon nanotube FET technology for radio-frequency electronics: state-of-the-art overview *IEEE J. Electron Devices Soc.* **1** 9–20

[92] Nougaret L *et al* 2009 80 GHz field-effect transistors produced using high purity semiconducting single-walled carbon nanotubes *Appl. Phys. Lett.* **94** 243505

[93] Krasnozhon D *et al* 2014 MoS_2 transistors operating at gigahertz frequencies *Nano Lett.* **14** 5905–11

[94] Radisavljevic B *et al* 2011 Single-layer MoS_2 transistors *Nat. Nanotechnol.* **6** 147–50

[95] Persson K-M *et al* 2013 Extrinsic and intrinsic performance of vertical InAs nanowire MOSFETs on Si substrates *IEEE Trans. Electron Devices* **60** 2761–7

[96] Johansson S *et al* 2014 High-frequency gate-all-around vertical InAs nanowire MOSFETs on Si substrates *IEEE Electron Device Lett.* **35** 518–20

[97] Egard M *et al* 2010 Vertical InAs nanowire wrap gate transistors with $f_T > 7$ GHz and $f_{max} > 20$ GHz *Nano Lett.* **10** 809–12

[98] Vandenbrouck S *et al* 2009 12 GHz f_{max} GaN/AlN/AlGaN nanowire MISFET *IEEE Electron Device Lett.* **30** 322–4

[99] Dattoli E N *et al* 2009 Radio-frequency operation of transparent nanowire thin-film transistors *IEEE Electron Device Lett.* **30** 730–2

[100] Takahashi T *et al* 2010 Parallel-array InAs nanowire transistors for mechanically bendable, ultrahigh frequency electronics *ACS Nano* **4** 5855–60

[101] Gu J *et al* 2011 First experimental demonstration of gate-all-around III–V MOSFETs by top-down approach *Proc. of the IEEE Int. Electron Devices Meeting* pp 33.2.1–4

[102] Xie P *et al* 2009 Diameter-dependent dopant location in silicon and germanium nanowires *Proc. Natl Acad. Sci.* **106** 15254–8

[103] Casadei A *et al* 2013 Doping incorporation paths in catalyst-free Be-doped GaAs nanowires *Appl. Phys. Lett.* **102** 013117

[104] Tomioka K, Yoshimura M and Fukui T 2012 A III–V nanowire channel on silicon for high-performance vertical transistors *Nature* **488** 189–92

[105] Morkotter S *et al* 2015 Demonstration of confined electron gas and steep-slope behavior in delta-doped GaAs–AlGaAs core–shell nanowire transistors *Nano Lett.* **15** 3295–302

[106] Dambrine G *et al* 1988 A new method for determining the FET small-signal equivalent circuit *IEEE Trans. Microw. Theory Tech.* **36** 1151–9

[107] Berroth M and Bosch R 1990 Broad-band determination of the FET small-signal equivalent circuit *IEEE Trans. Microw. Theory Tech.* **38** 891–5

[108] Brady R G, Oxley C H and Brazil T J 2008 An improved small-signal parameter-extraction algorithm for GaN HEMT devices *IEEE Trans. Microw. Theory Tech.* **56** 1535–44

[109] Choi W *et al* 2017 Direct electrical probing of periodic modulation of zinc-dopant distributions in planar gallium arsenide nanowires *ACS Nano* **11** 1530–9

[110] Dowdy R S *et al* 2013 Perturbation of Au-assisted planar GaAs nanowire growth by p-type dopant impurities *Opt. Mater. Express* **3** 1687–97

[111] Qu J *et al* 2016 Direct observation of dopants distribution and diffusion in GaAs planar nanowires with atom probe tomography *ACS Appl. Mater. Interfaces* **8** 26244–50